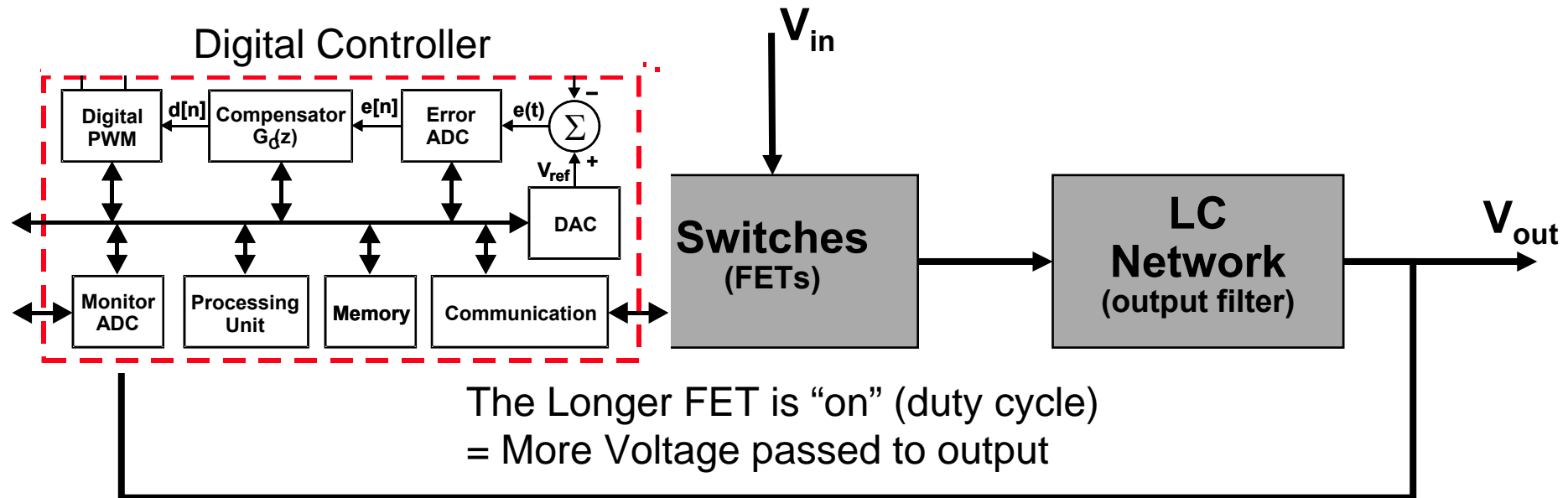


C2000 Digital Power Solutions

Agenda

- Power Systems Overview
- Why Digital Control
- Digital Controller Requirements
- Why C2000 for Digital Power
- Software Development Tools
- Hardware Development Tools

Voltage Regulator Systems



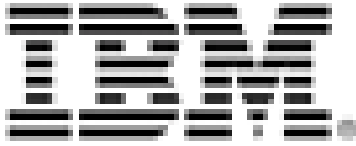
Goal: Maintain constant V_{out} regardless of change in V_{in} or load, within spec.

The controller block is what differentiates between a digital power system and a conventional analog power system

Agenda

- Power Systems Overview
- Why Digital Control
- Digital Controller Requirements
- Why C2000 for Digital Power
- Software Development Tools
- Hardware Development Tools

Why Move to Digital?



Powercasts © 2006 Darnell Group, Inc.

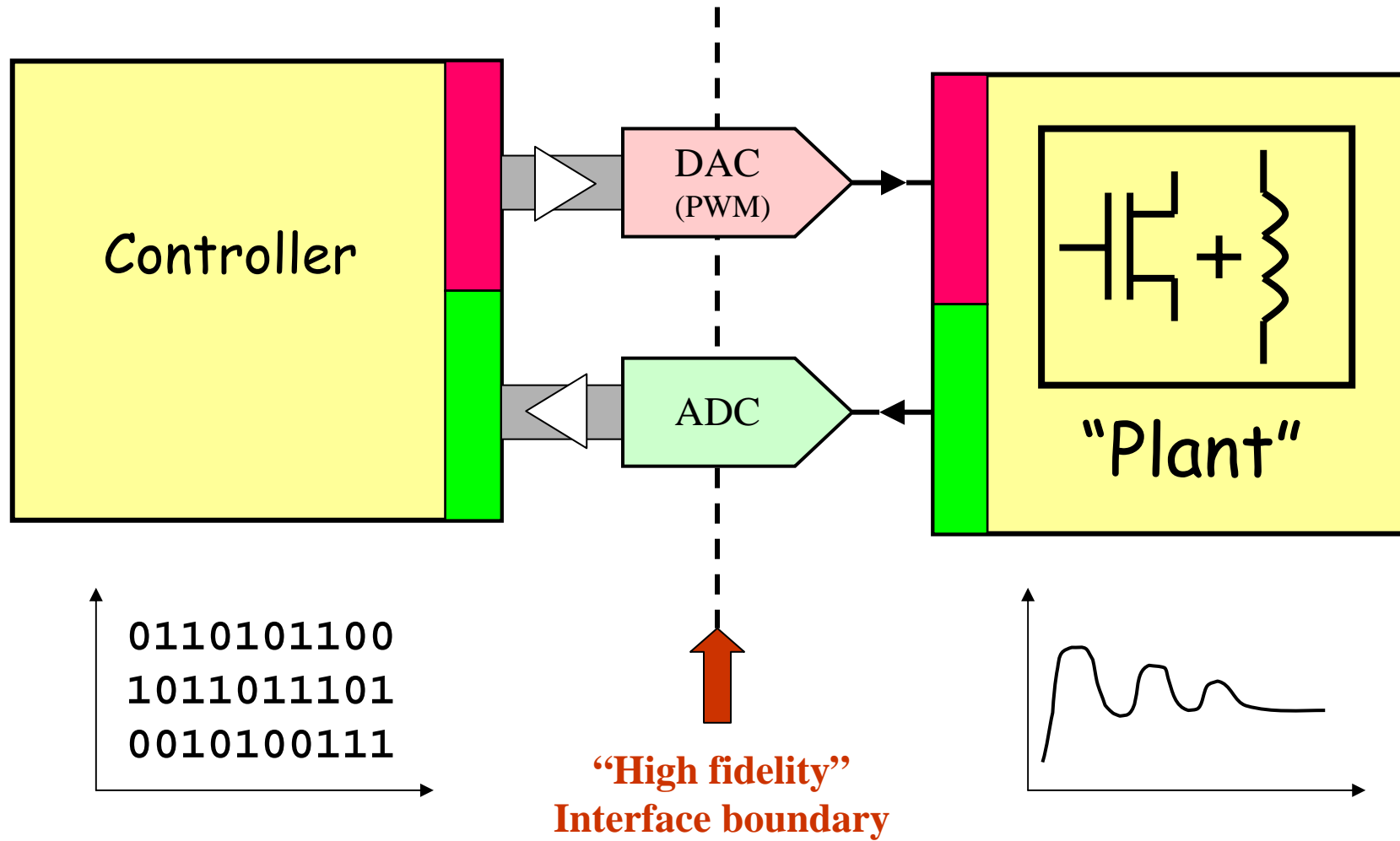
Wants their server power suppliers to because it...

- Reduces Costs
 - Development
 - Tunable Platforms Lead to New Products Quicker
 - Qualification
 - Calibration, better noise and temperature immunity
 - Manufacturing
 - Reduced Board Area
 - Reduced Parts Count = Lower Inventory
- Higher Quality
 - Adaptive; efficiency across load range
 - Flexibility Through Programmability
 - Calibration at Final Functional Test
 - Less Sensitive to Environment and Component Drift
 - Better Noise Immunity
 - Parameter Monitoring for Continual Quality Improvement
- Higher Reliability
 - Intelligent Diagnostics, Failure Prediction; Reporting Capability
 - Reduced Parts Count = Fewer Field Failures

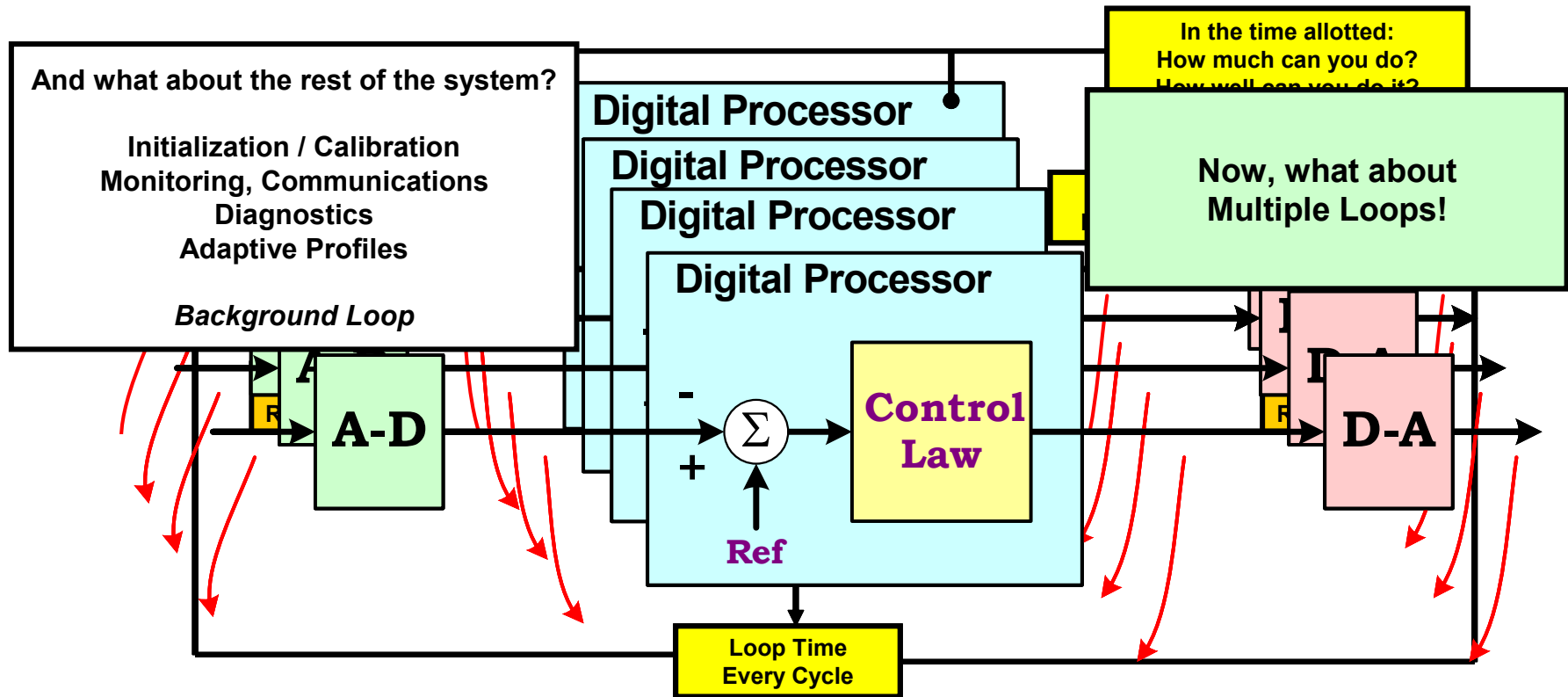
Agenda

- Power Systems Overview
- Why Digital Control
- **Digital Controller Requirements**
- Why C2000 for Digital Power
- Software Development Tools
- Hardware Development Tools

Digitally Controlled System

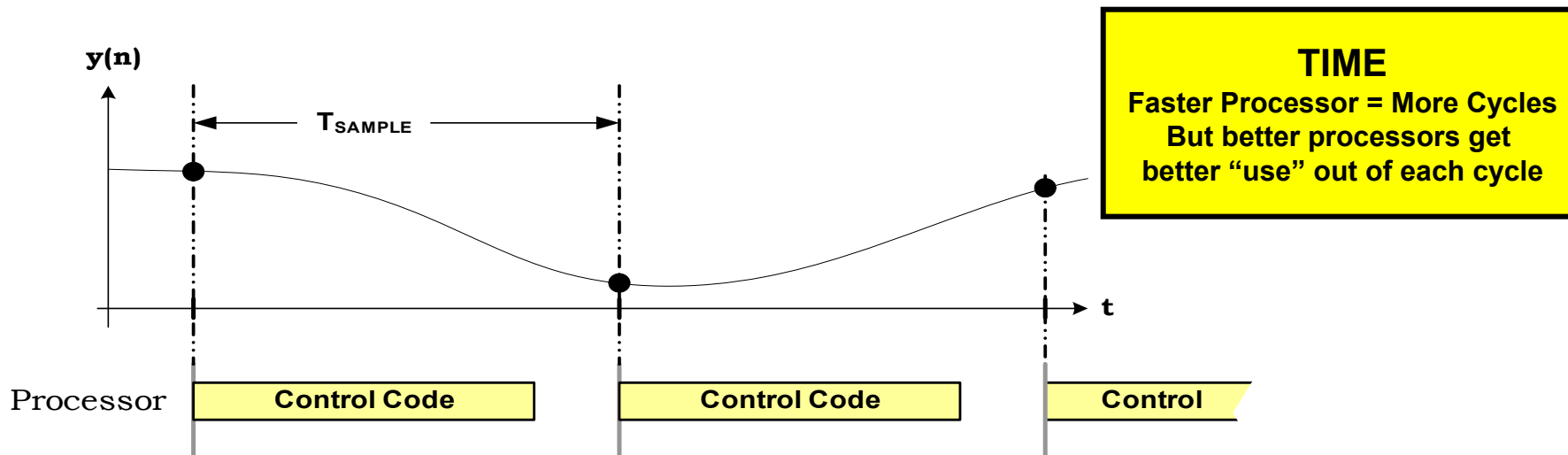


Time Sampled Systems What Matters?



You need to sample-control-output i.e. "close the loop" within the sample period T .
Sample Period = Frequency of System Update
Faster Sampling = Better Control!

Time: How much do you get?



- The system control signals must be updated at a specific rate, or sample frequency
- In a digital system the controller must read in a sample, process it, and then send out updated control signals
 - This requires that the controller execute the control code faster than the sample frequency
- *The faster the sample frequency, the less time the processor has to execute the control code.*

Control Loop Execution Times

- Digital power systems typically operate much faster than a motor control system
 - This is because faster sampling frequencies allow higher switching frequencies
 - Higher switching frequencies enable more efficiency and smaller electrical components
- Fast loop speeds make digital power very processor intensive

TIME
 Faster Processor = More Cycles
 But better processors get better “use” out of each cycle

| | Sample F = KHz | Period ns | Cycles @ 40 MHz | Cycles @ 60 MHz | Cycles @ 100 MHz | Cycles @ 300 MHz |
|---------------|-------------------|--------------|--------------------|--------------------|---------------------|---------------------|
| Motor Control | 10 | 100,000 | 4,000 | 6,000 | 10,000 | 30,000 |
| | 20 | 50,000 | 2,000 | 3,000 | 5,000 | 15,000 |
| PFC AC/DC | 50 | 20,000 | 800 | 1,200 | 2,000 | 6,000 |
| | 100 | 10,000 | 400 | 600 | 1,000 | 3,000 |
| DC/DC | 250 | 4,000 | 160 | 240 | 400 | 1,200 |
| | 500 | 2,000 | 80 | 120 | 200 | 600 |
| | 1,000 | 1,000 | 40 | 60 | 100 | 300 |
| | 1,500 | 667 | 27 | 40 | 67 | 200 |
| | 2,000 | 500 | 20 | 30 | 50 | 150 |

What do you spend this time on?

- Sample Frequency = execution time for control loop
 - Interrupts / Latency
 - ADC Sampling / Converting
 - Control / Compensation
 - Ex: 2nd order Look-Up Table, Direct-Form Digital Filter, PI / PID Digital Filter, 2P2Z, 3P3Z
 - PWM Driver (Pattern Generation)
 - Ex: Buck, Phase Shifted Full Bridge, PFC, 2 Phase Interleaved, Multi-phase Interleaved, Half H-Bridge, Full Bridge, DAC, etc
 - *Processor must be able to execute loop faster than the sample frequency*
- Extra cycles are spent running background tasks or other control loops
 - Communications, sequencing, margining, fault detection, “secret sauce”
 - *Control loop execution time directly affects what other tasks the processor can run*

TIME

What can you do?

TIME

How well can you do it?

To be discussed in the software section...

Background Loop

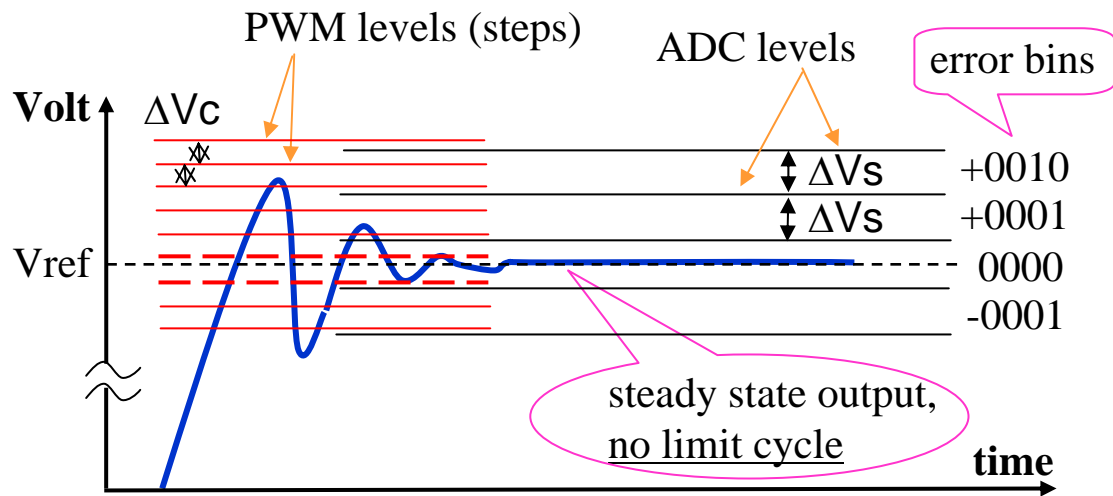
- Cycles not used by the control loop are used in the background task
- Background tasks encompass digital communication to report status, fault, and on-line diagnostics. Other possibilities are:
 - Dynamic configuration
 - Margining
 - Soft start/stop
 - Tracking
 - Sequencing
 - Synchronization
 - Selectable fault response
 - Output voltage set-point
 - Load current monitoring
 - Temperature monitoring
 - OC, OV, and OT protection threshold programming
 - Power Good, Critical Fault Indicators
 - Error data logging to flash or through comms
- *Background tasks enable customer's "special sauce" that differentiates from competitors*



Good PWM Resolution

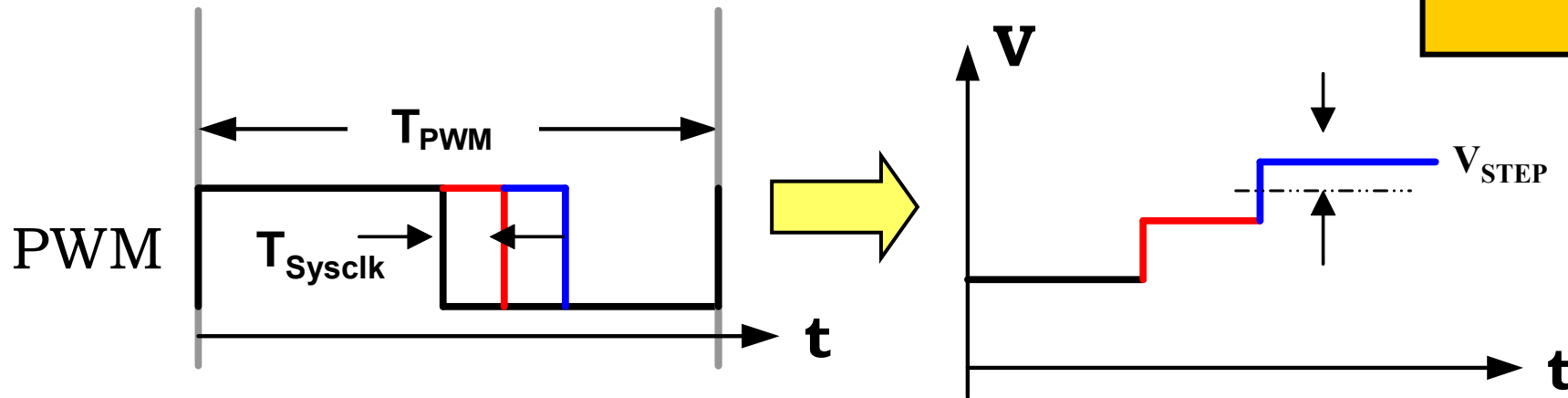
Output Resolution

- High resolution on the PWM output enables more “steps” enabling the controller to hit the desired output
 - *PWM steps typically correspond to duty cycle, other PWM characteristics can also affect the system.*
- Typically to have enough resolution the system’s DAC resolution must be greater than the ADC resolution



DAC Resolution: PWM Steps

Output Resolution



$$\text{DAC Resolution} = \log_2 (\text{Period} / \text{Step-Size})$$

| Update Period (kHz) | PWM Step | |
|------------------------|-----------------|-----------------|
| | 25 ns (bits) | 10 ns (bits) |
| 20 | 11.0 | 12.3 |
| 50 | 9.6 | 11.0 |
| 100 | 8.6 | 10.0 |
| 150 | 8.1 | 9.4 |
| 250 | 7.3 | 8.6 |
| 500 | 6.3 | 7.6 |
| 750 | 5.7 | 7.1 |
| 1000 | 5.3 | 6.6 |
| 1500 | 4.7 | 6.1 |
| 2000 | 4.3 | 5.6 |

- PWM step size is based on the PWM clock, which is usually derived from the CPU clock
 - 40 MHz Clock = 25 ns Step
 - 100 MHz Clock = 10 ns Step
- Minimum PWM resolution needs to be ≥ 10 bits
- For high frequency loops standard PWM gives too little resolution

DAC Resolution: High-Res PWM

Output Resolution

- At 20MHz almost any power stage can be controlled
- At a resolution of 150 pico seconds frequencies over 20MHz can be achieved
 - To reach the frequency with a traditional PWM the clock would need to be over 6.6GHz!
- High resolution PWM technology from TI enables 150ps resolution off of a 40MHz clock*

| Update Period (kHz) | PWM Step | | |
|------------------------|-----------------|-----------------|------------------|
| | 25 ns (bits) | 10 ns (bits) | 150 ps (bits) |
| 20 | 11.0 | 12.3 | 18.3 |
| 50 | 9.6 | 11.0 | 17.0 |
| 100 | 8.6 | 10.0 | 16.0 |
| 150 | 8.1 | 9.4 | 15.4 |
| 250 | 7.3 | 8.6 | 14.7 |
| 500 | 6.3 | 7.6 | 13.7 |
| 750 | 5.7 | 7.1 | 13.1 |
| 1000 | 5.3 | 6.6 | 12.7 |
| 1500 | 4.7 | 6.1 | 12.1 |
| 2000 | 4.3 | 5.6 | 11.7 |

What's Important for a Digital Controller

1. High speed control loop execution

- Processor must be able to execute control loop faster than the system update frequency
- Processor needs to execute control code fast enough to leave headroom for background tasks

2. High fidelity analog to digital and digital to analog conversion

- High speed, good resolution ADC
- High resolution PWM output

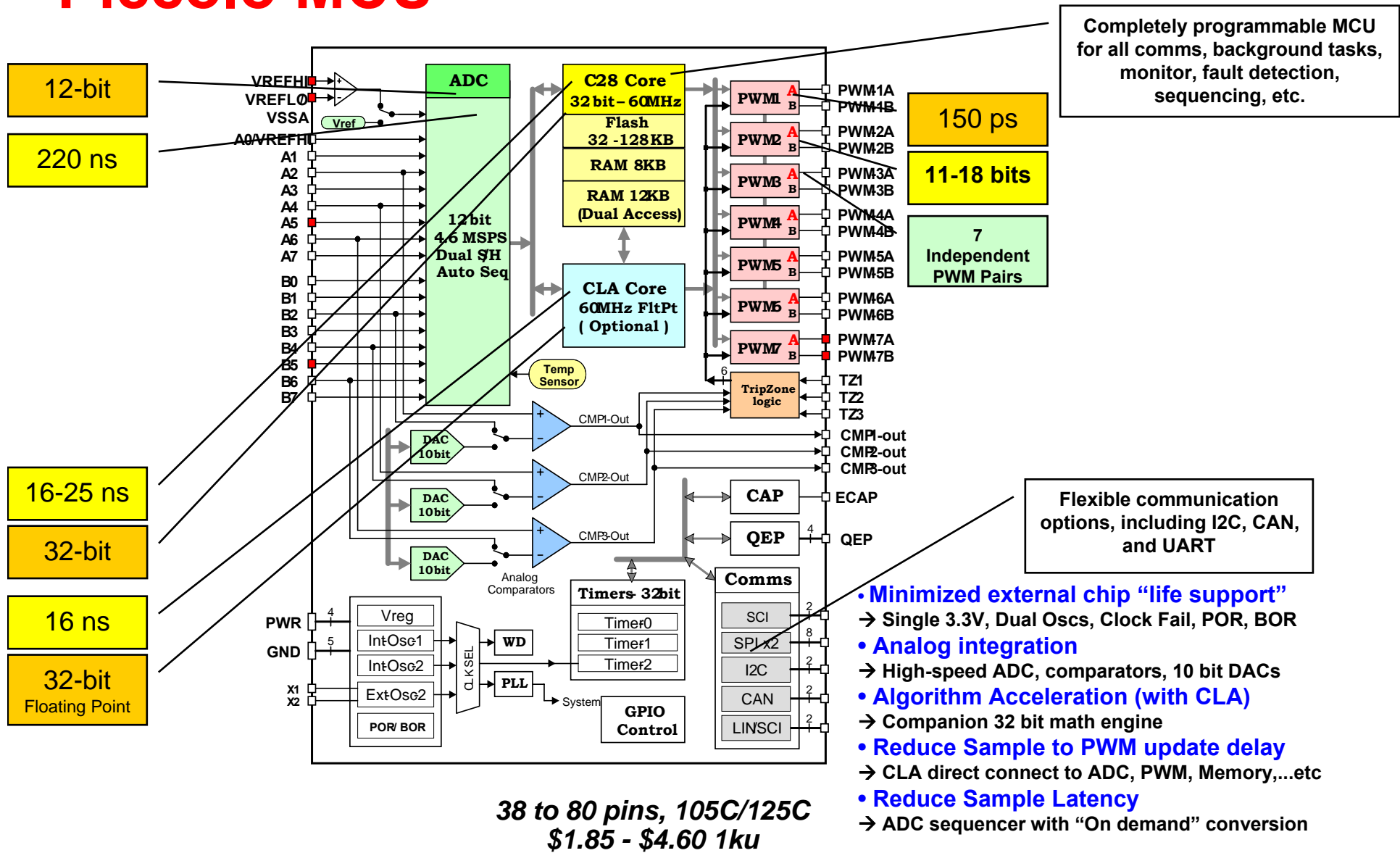
3. Software

- Since the system is being controlled digitally, software to control the system must be written
- Customers need example code, libraries, and easy to use development tools

Agenda

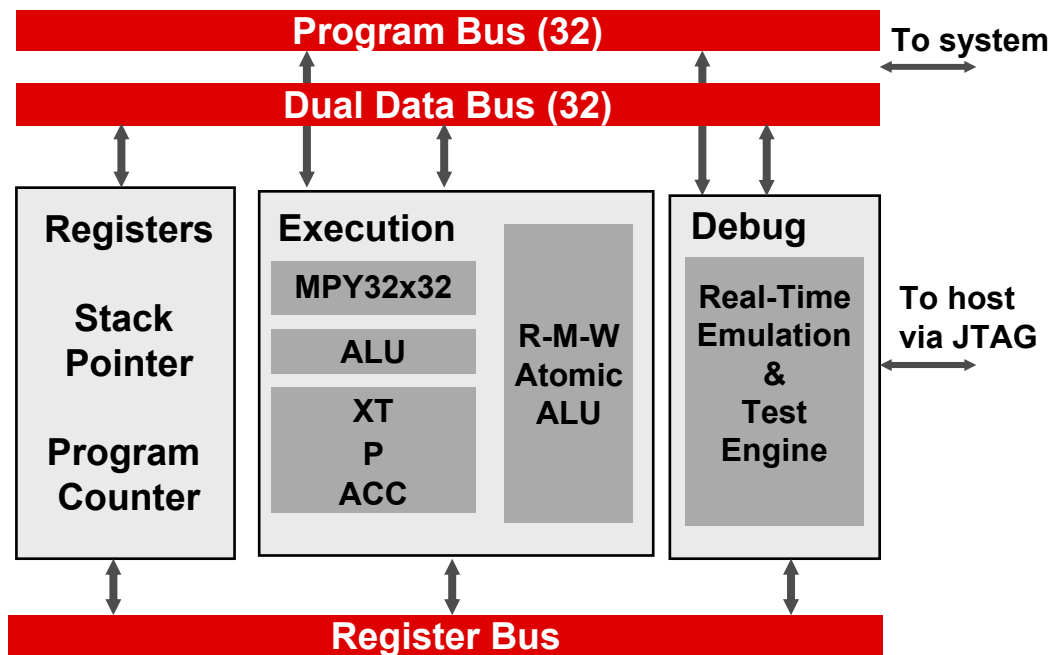
- Power Systems Overview
- Why Digital Control
- Digital Controller Requirements
- Why C2000 for Digital Power
- Software Development Tools
- Hardware Development Tools

Piccolo MCU



C28x Core

The 32-bit C28x core is at the heart of every C2000 28x microcontroller. Based on a DSP architecture, the core is optimized to quickly execute math-based operations, but can also handily process general-purpose code.



C28x CPU

- 32-bit fixed-point DSP
- RISC instruction set
- 8-stage protected pipeline
- 32x32 bit fixed-point MAC for single-cycle 32-bit multiplies
- Dual 16x16 bit fixed-point MACs
- Single-cycle instruction execution

Modified Harvard Bus Architecture

- Separate data and instruction buss
- Two data buses – one for read, one for write
- Enables fetch, read, and write in a single cycle

Emulation Logic

- Real-time emulation allows interrupt servicing even when main program is halted
- Debug host has direct access to registers and memory
- Enables data logging to the debug host
- Multiple hardware debug events and breakpoints

Control Law Accelerator (CLA)

Independent 32-bit floating-point math accelerator

Operates independently of the C28x CPU

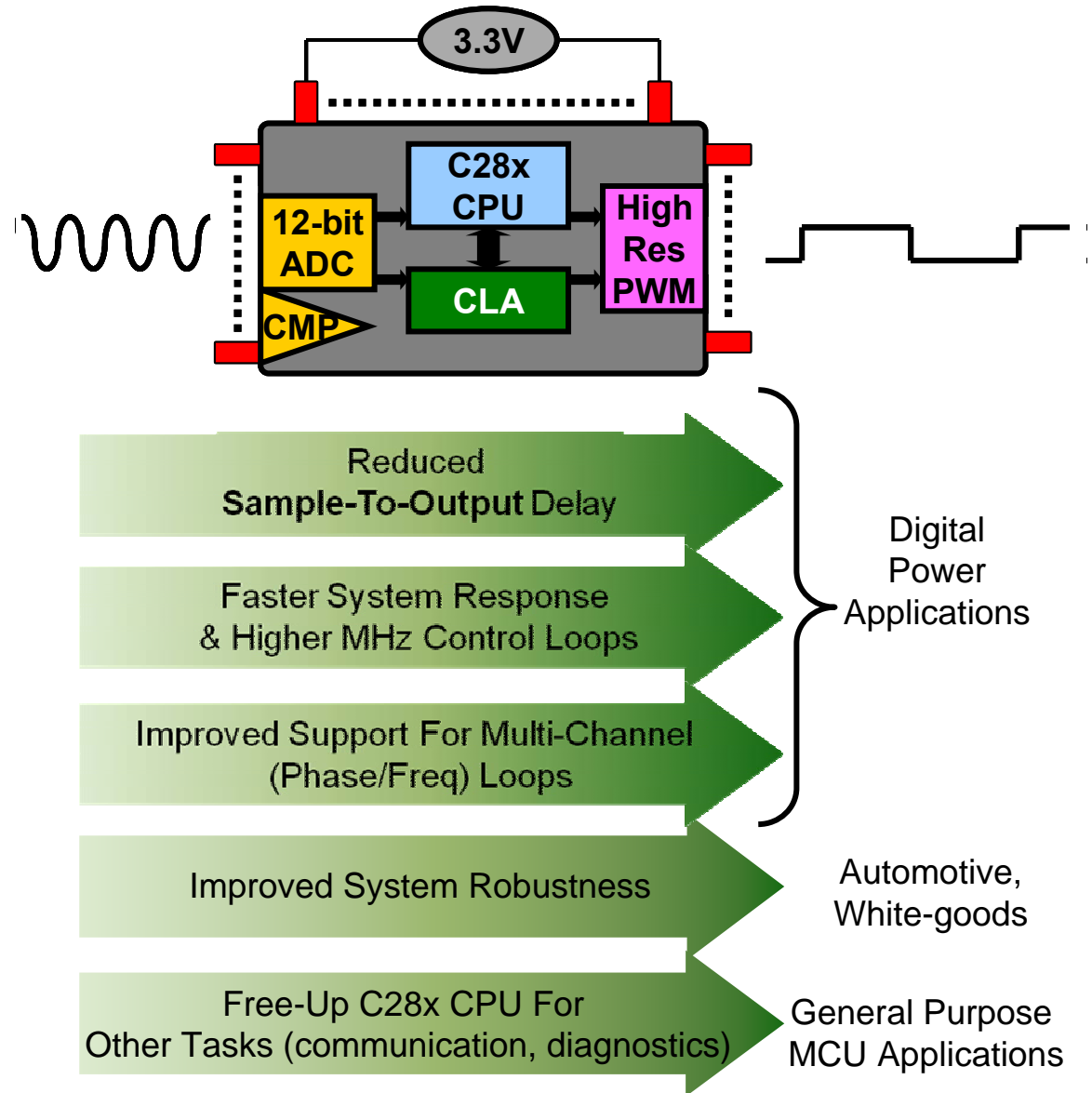
- Independent register set, memory bus structure & processing unit
- Low interrupt response time

Direct access to on-chip peripherals

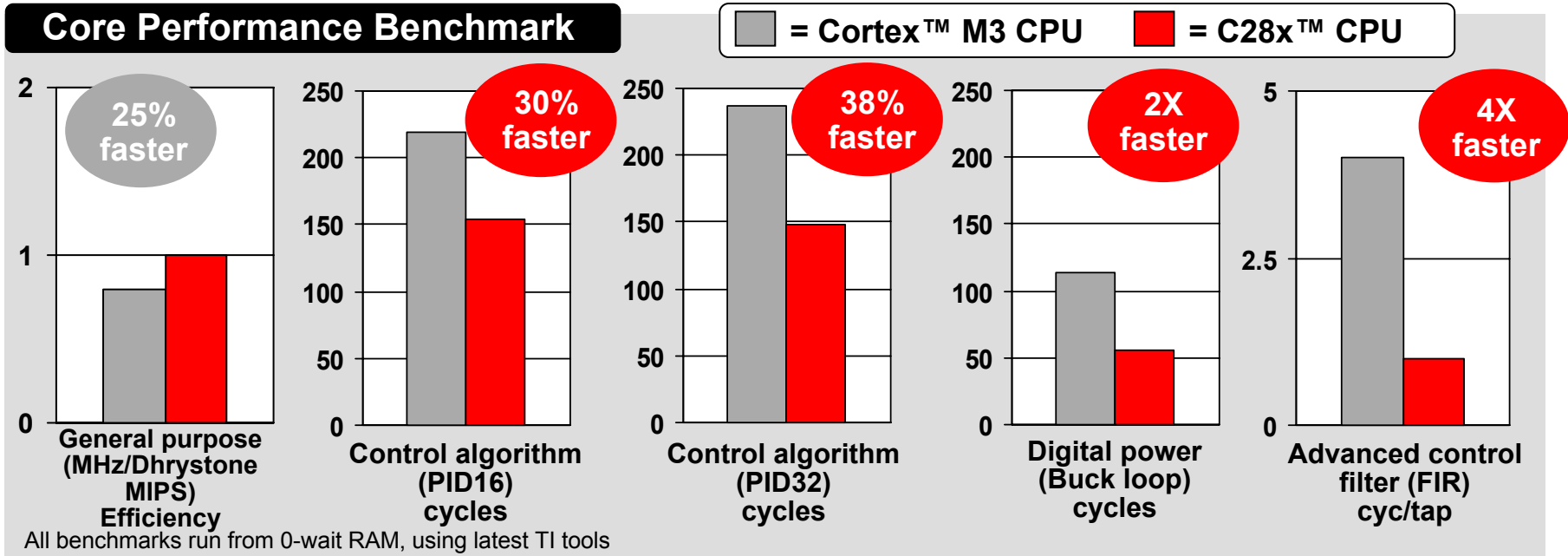
- Execution of algorithms in parallel with the C28x CPU

Fully programmable: IEEE 32-bit floating

- Removes scaling and saturation burden



Piccolo™ is the right solution for Real-Time Control



| Operation | Cortex-M3 (72 MHz) | C28 (60MHz) | C28/CLA (60MHz) |
|-------------------------------|--------------------|---------------|------------------|
| Feedforward control cycles | 786 | 482 | 482 / 0 |
| Feedback control cycles | 1762 | 1081 | 0 / 550 |
| Total Control Law cycles | 2548 | 1563 | 482 / 550 |
| MHz used (20 kHz loop) | ~51MHz | ~32MHz | ~10/11MHz |

Dhrystone benchmark is industry standard, does not benchmark the math performance of a processor

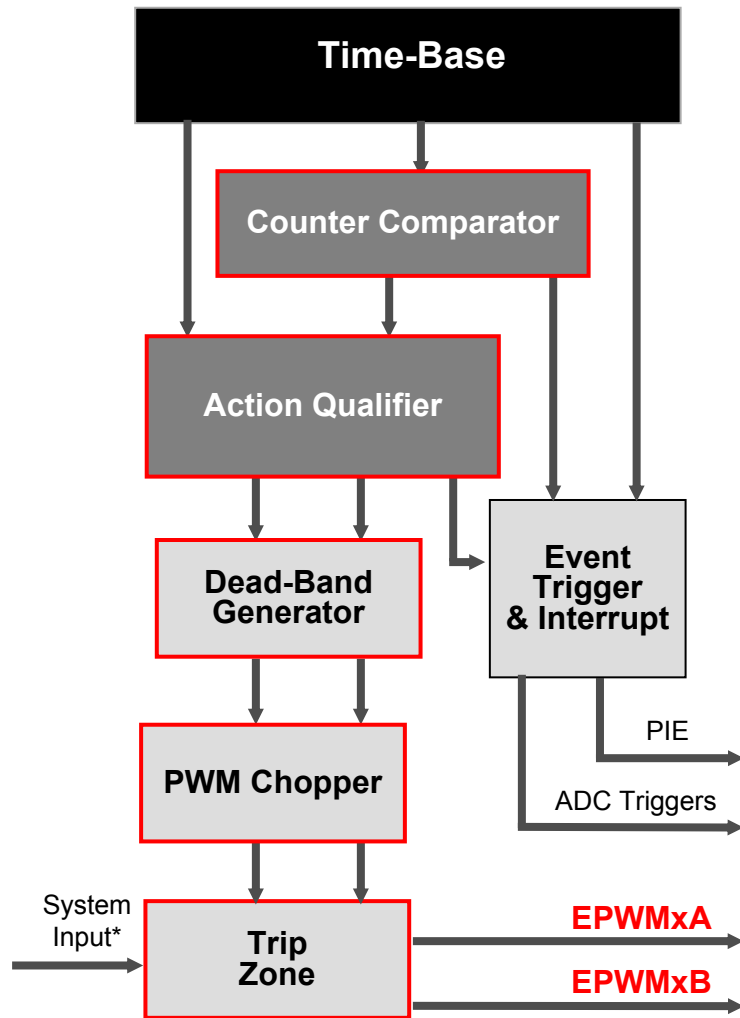
< 1/3 headroom

20% faster, lower frequency, 50% headroom

5X faster, lower frequency 80% headroom

Enhanced PWM (ePWM)

Each ePWM module has two independently configurable outputs, EPWMxA and EPWMxB, as illustrated below:



Dedicated 16-bit Time Base

- Uses prescaled CPU system clock.
- Synchronizes with other ePWM Modules in phase shift and frequency

Counter Comparator (CC)

- Registers and comparators eliminate the need to interrupt the CPU in PWM generation
- Can function as a 16-bit input capture (rising edge only)

Action Qualifier

- Generates actual PWM signal with information from CC and timer.

Programmable Dead-Band Generator

- Programmable rising-edge and falling-edge delay

PWM Chopper

- Allows a high-frequency carrier signal to modulate PWM waveforms
- Programmable chopping frequency, duty cycle, and first pulse width

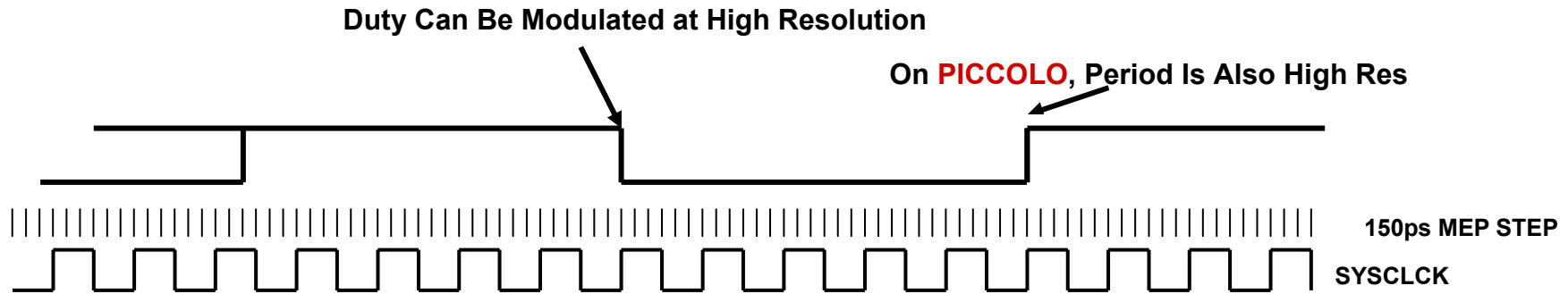
Programmable Trip Zone Generator

- Quickly overrides PWM signals to a pre-programmed state.
- One-shot or cycle-by-cycle operation
- Can generate events, filtered events, or trip conditions

Event Trigger and Interrupt

- Two ADC start-of-conversion signals and a PIE interrupt request line

High Resolution PWM



EX:

Target PWM f = 189.753KHz

50% Duty Cycle

40MHz SYSCLK

Hi-Res

189.755KHz, error = 2Hz = 0.001%

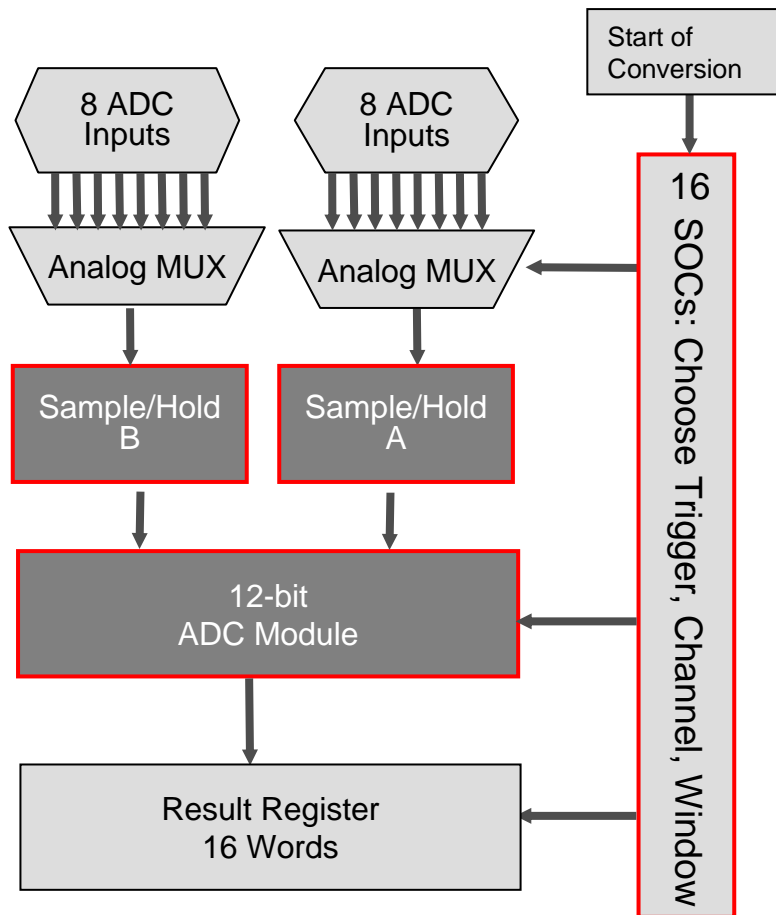
No Hi-Res

190.476KHz, error = 721Hz = 0.38%

| Update Period (kHz) | PWM Step | | |
|------------------------|-----------------|-----------------|------------------|
| | 25 ns (bits) | 10 ns (bits) | 150 ps (bits) |
| 20 | 11.0 | 12.3 | 18.3 |
| 50 | 9.6 | 11.0 | 17.0 |
| 100 | 8.6 | 10.0 | 16.0 |
| 150 | 8.1 | 9.4 | 15.4 |
| 250 | 7.3 | 8.6 | 14.7 |
| 500 | 6.3 | 7.6 | 13.7 |
| 750 | 5.7 | 7.1 | 13.1 |
| 1000 | 5.3 | 6.6 | 12.7 |
| 1500 | 4.7 | 6.1 | 12.1 |
| 2000 | 4.3 | 5.6 | 11.7 |

12-bit Pipeline/SAR Hybrid ADC

Piccolo's hybrid ADC allows flexible creation of conversion sequences.



Start of Conversion (SOC) Configuration and Logic Block

- 16 SOC triggers from Software, CPU timers, ePWMs, and GPIOs
- Allows easy creation of conversion sequences
- Multiple conversions can be processed in Round Robin or Priority Modes
- 9 flexible interrupts

Up to 16 Analog Inputs

- 16 channel, multiplexed analog inputs.
- Supports both 0-3.3V fixed range and ratio-metric input range

Analog Mux

- Uses SOC input to select which channels will be processed

Dual Sample and Hold

- Dual sample/hold enable simultaneous sampling or sequencing sampling modes
- Adjustable acquisition window ensures proper sampling

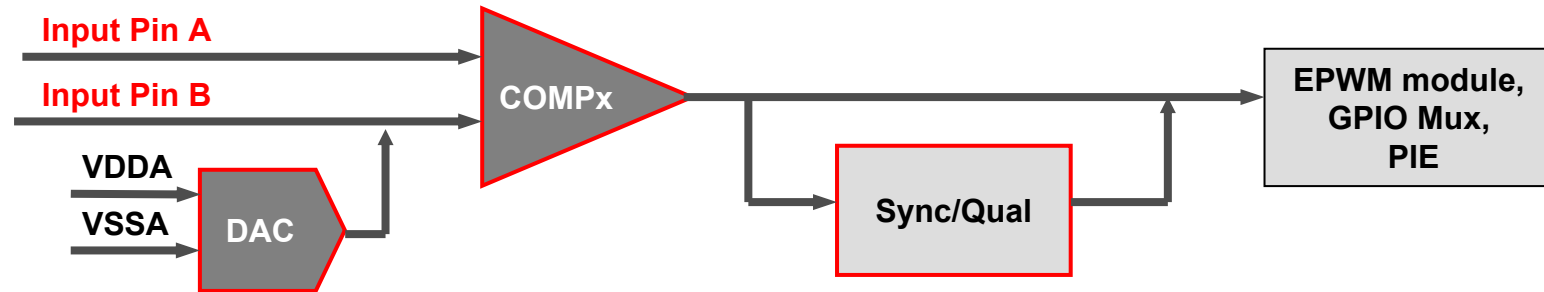
12-bit Analog-Digital Converter

- Fast conversion rate: Up to 5MSPS
- Just-in-time interrupts (early interrupts) eliminates context switch latency by calling interrupts before conversion finishes

Result Registers

- Sixteen result registers (individually addressable) to store conversion values

Comparators



- Comparators enable instant protection in the case of a fault condition
 - Example: Output is shorted, system starts to draw too much current. Current measurement fed directly to the comparator. Once too much current is drawn comparator instantly shuts off PWMs shutting down the system
- 30ns response time to PWM modules
- Comparator can also be used for Peak Current Control
- For more information see “C2000 Architecture and Peripherals” presentation

Comparator Reference Guide

Piccolo: F2802x, F2803x – [spruge5](#)

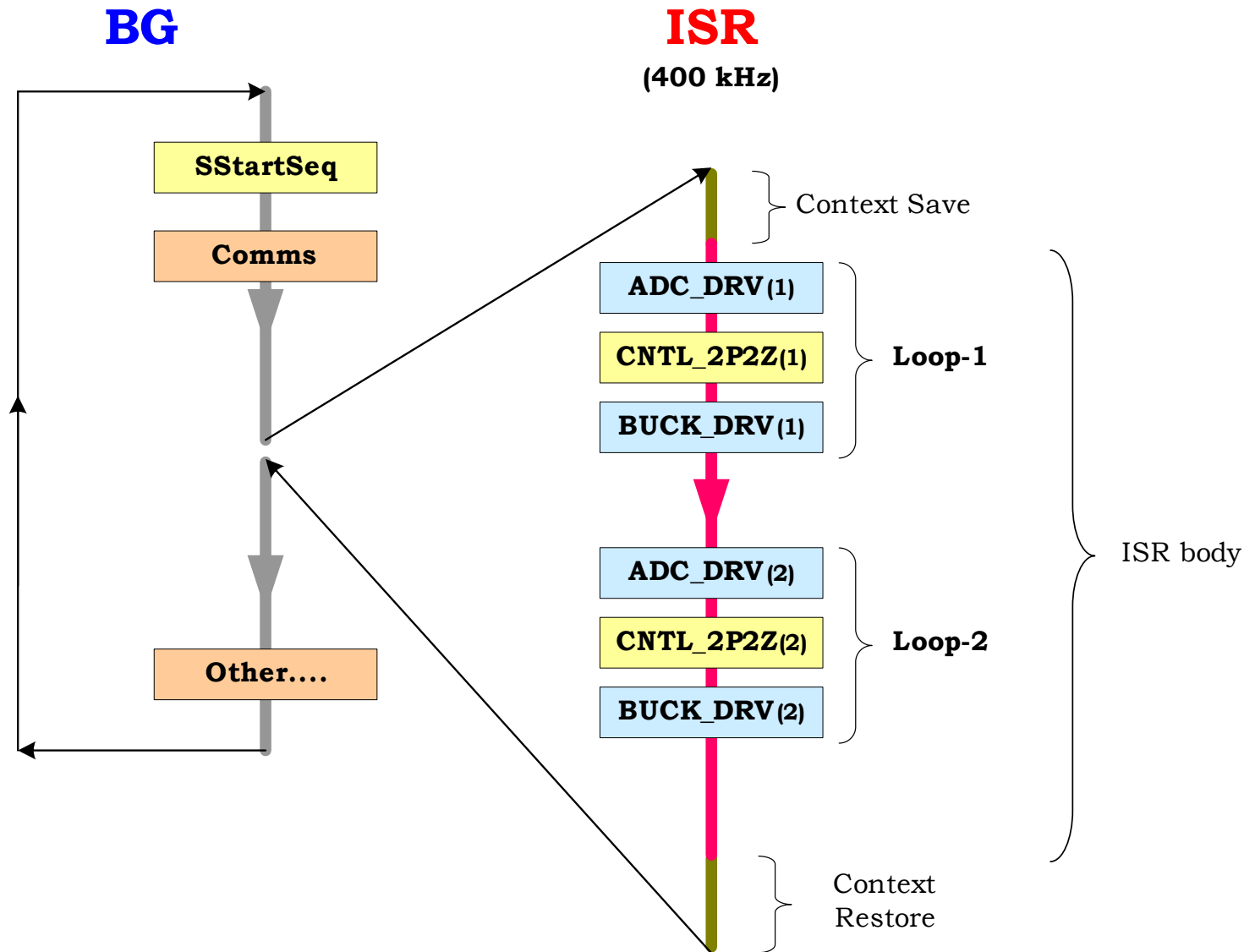
Agenda

- Power Systems Overview
- Why Digital Control
- Digital Controller Requirements
- Why C2000 for Digital Power
- **Software Development Tools**
- Hardware Development Tools

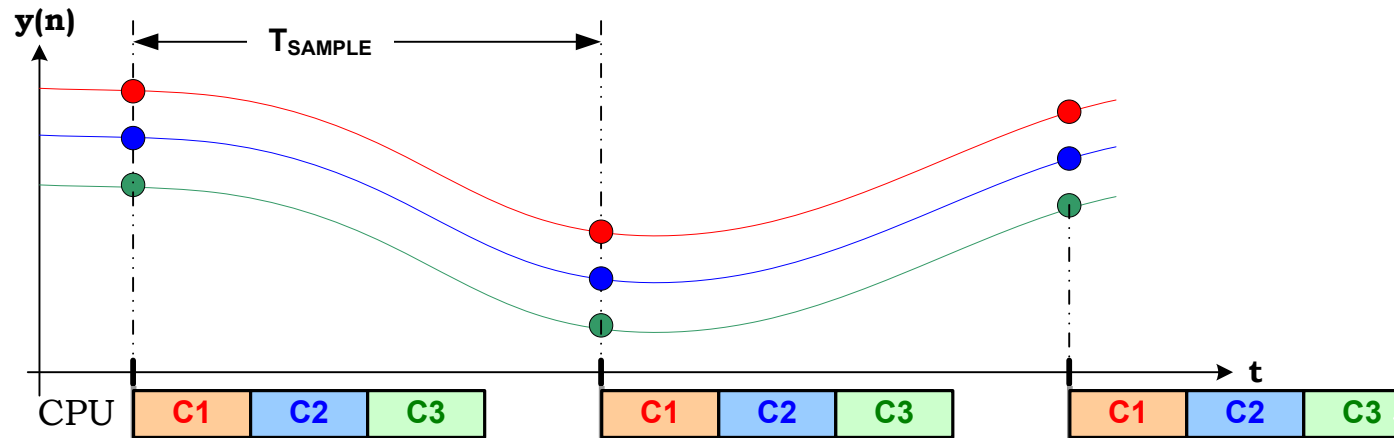
Control Software Basics

- Typically want to have one control loop interrupt and multiple background tasks
 - Single control loop interrupt runs all control loops
 - Enables software to be simple and loop execution time to be very deterministic
- For multiple control loop, the control loop interrupt runs at the speed of the fastest loop and the other loops are divided into sections
- Background loop runs all other tasks and services non-control (lower priority) interrupts
- This is TI's method for control software, some customers use and RTOS or other control schemes. The key is that the control loops must execute at a precise rate.

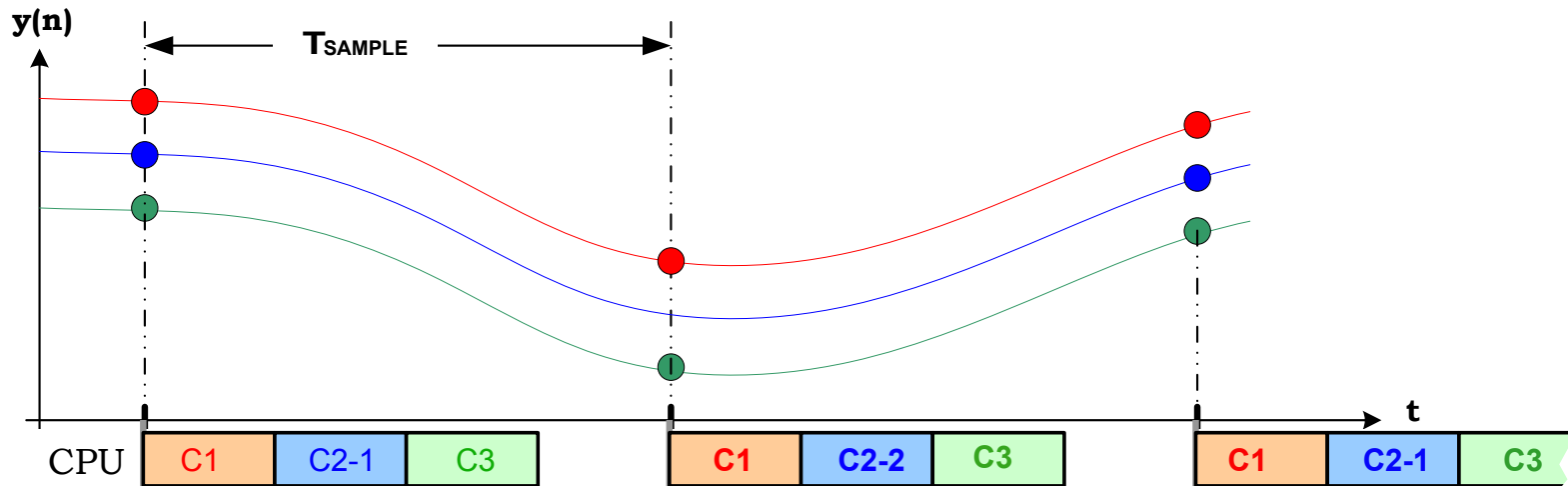
Software Structure



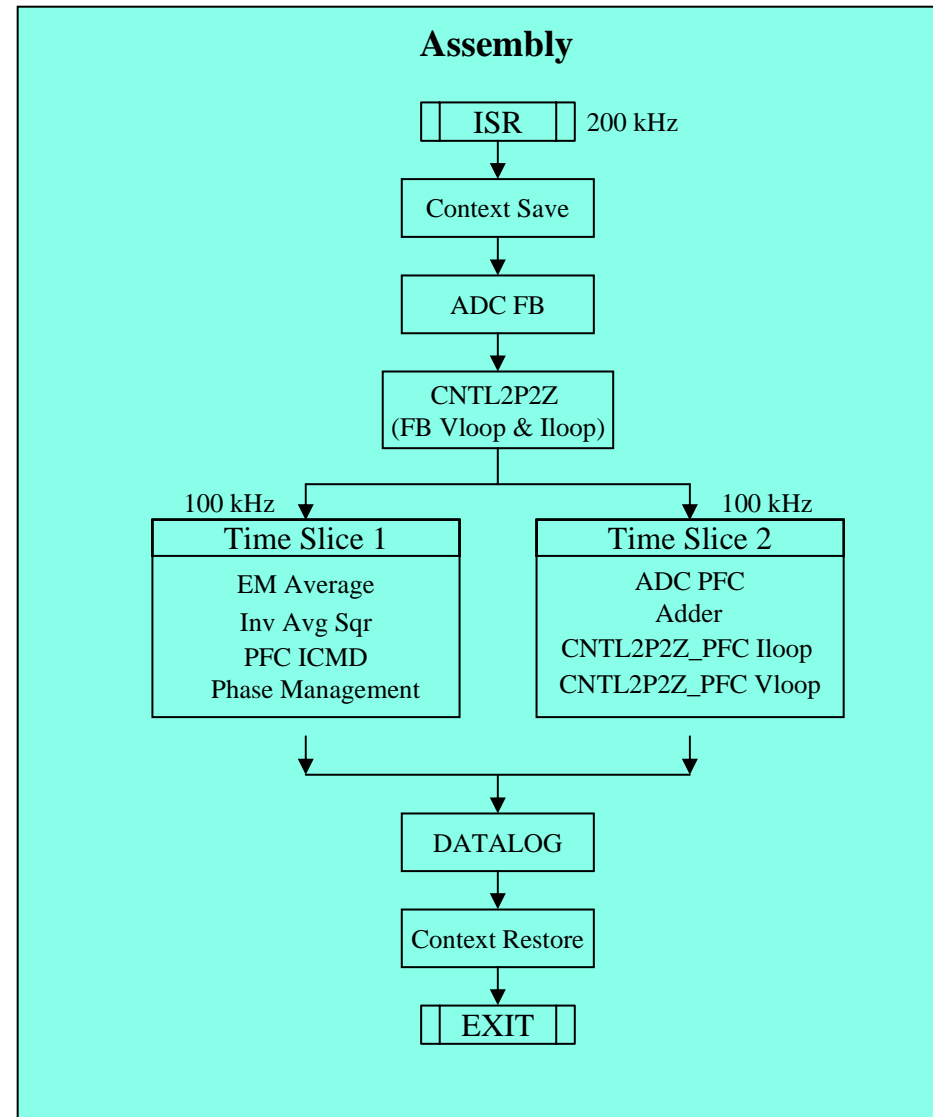
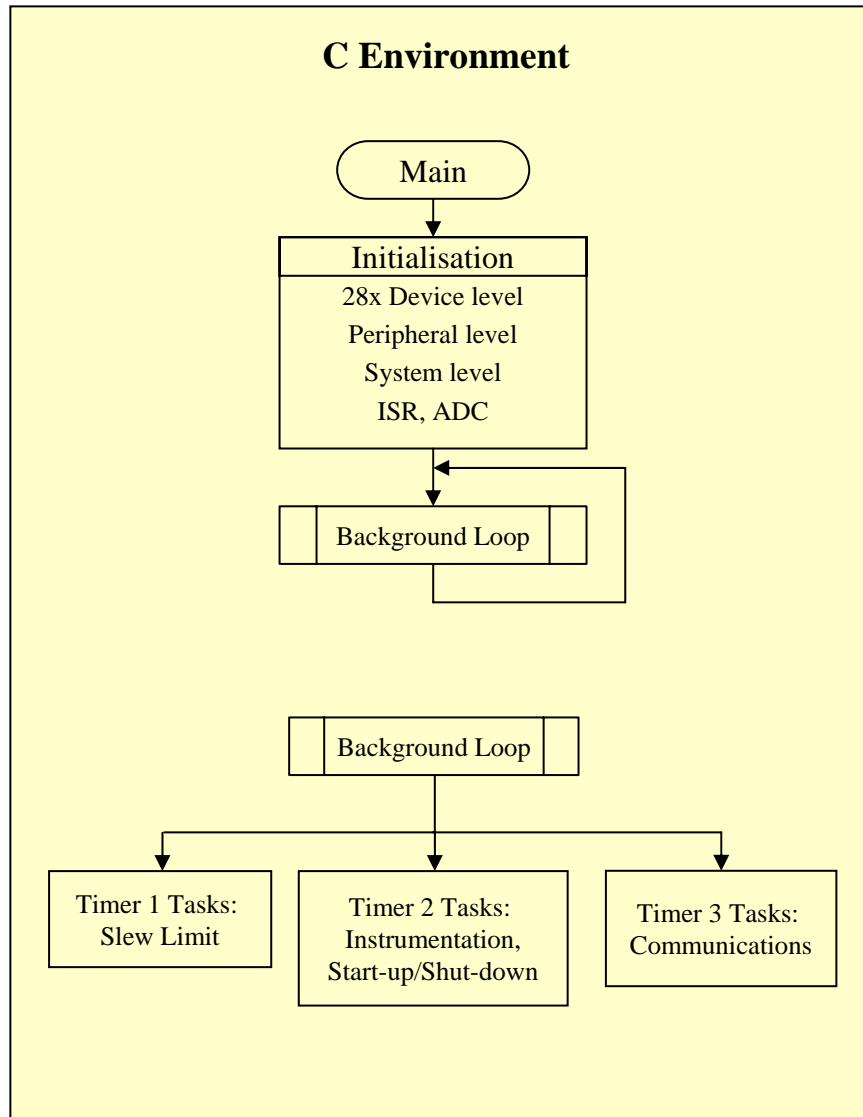
Running Multiple Loops



If you can close all the loops in a single Sample Time, GREAT!
If you can't, consider multiple Sample/Update Rates. Slower loops as a divisor of your fastest loop.
Time Division Multiplexing



Example: Rectifier Software

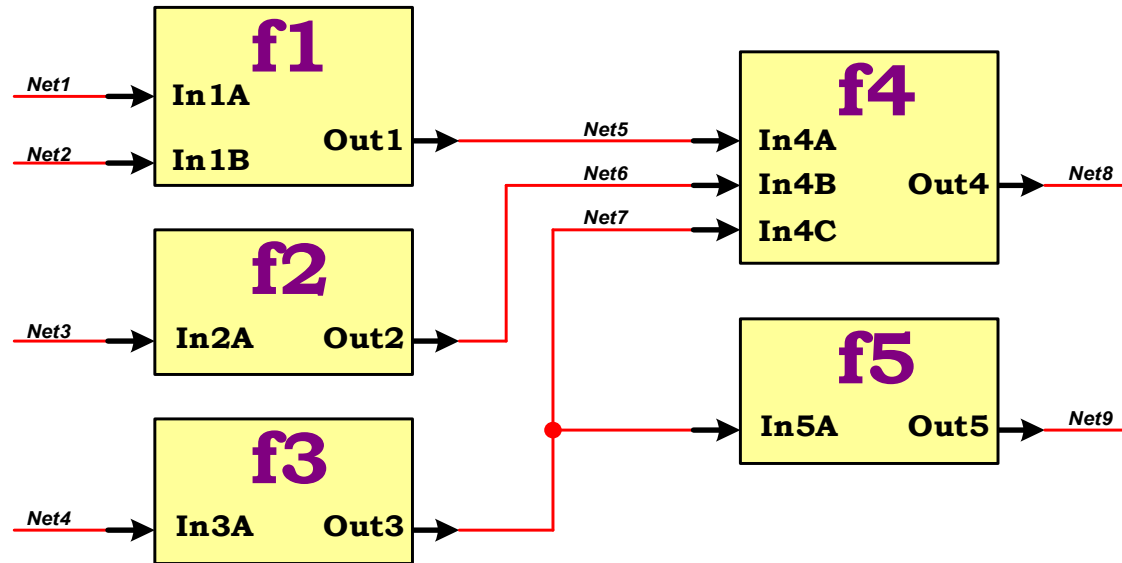


Software Examples and Libraries

- TI's controlSUITE software platform includes examples and modular software libraries
 - With one download controlSUITE provides all digital power software and libraries for C2000 MCUs
- Digital power library uses a modular software approach, with each part of the system being an easy to use software block
 - Over 20 blocks for the C2000 CPU and the CLA
 - Digital power library includes detailed documentation for each block
 - Modular approach enables easy software development

Modular SW Architecture

“Signal Net” based module connectivity



Initialization time

```
// pointer & Net declarations
Int *In1A, *In1B, *Out1, *In2A, ...
Int Net1, Net2, Net3, Net4, ...
```

```
// "connect" the modules
```

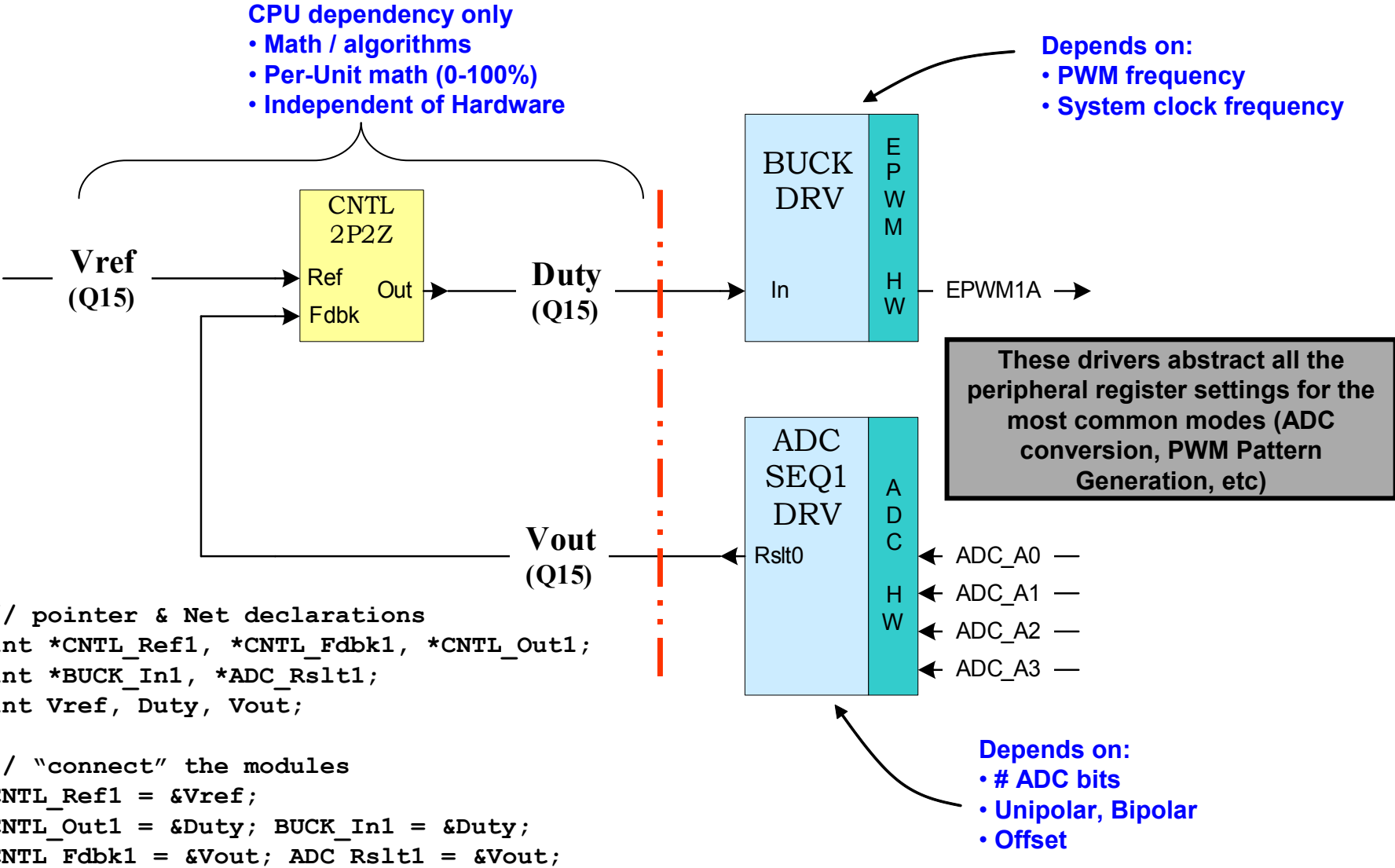
```
In1A=&Net1; In1B=&Net2; In2A=&Net3; In3A=&Net4; // inputs
Out4=&Net8; Out5=&Net9; // outputs
Out1=&Net5; In4A=&Net5; // Net5
Out2=&Net6; In4B=&Net6; // Net6
Out3=&Net7; In4C=&Net7; In5A=&Net7; // Net7
```

Run time - ISR

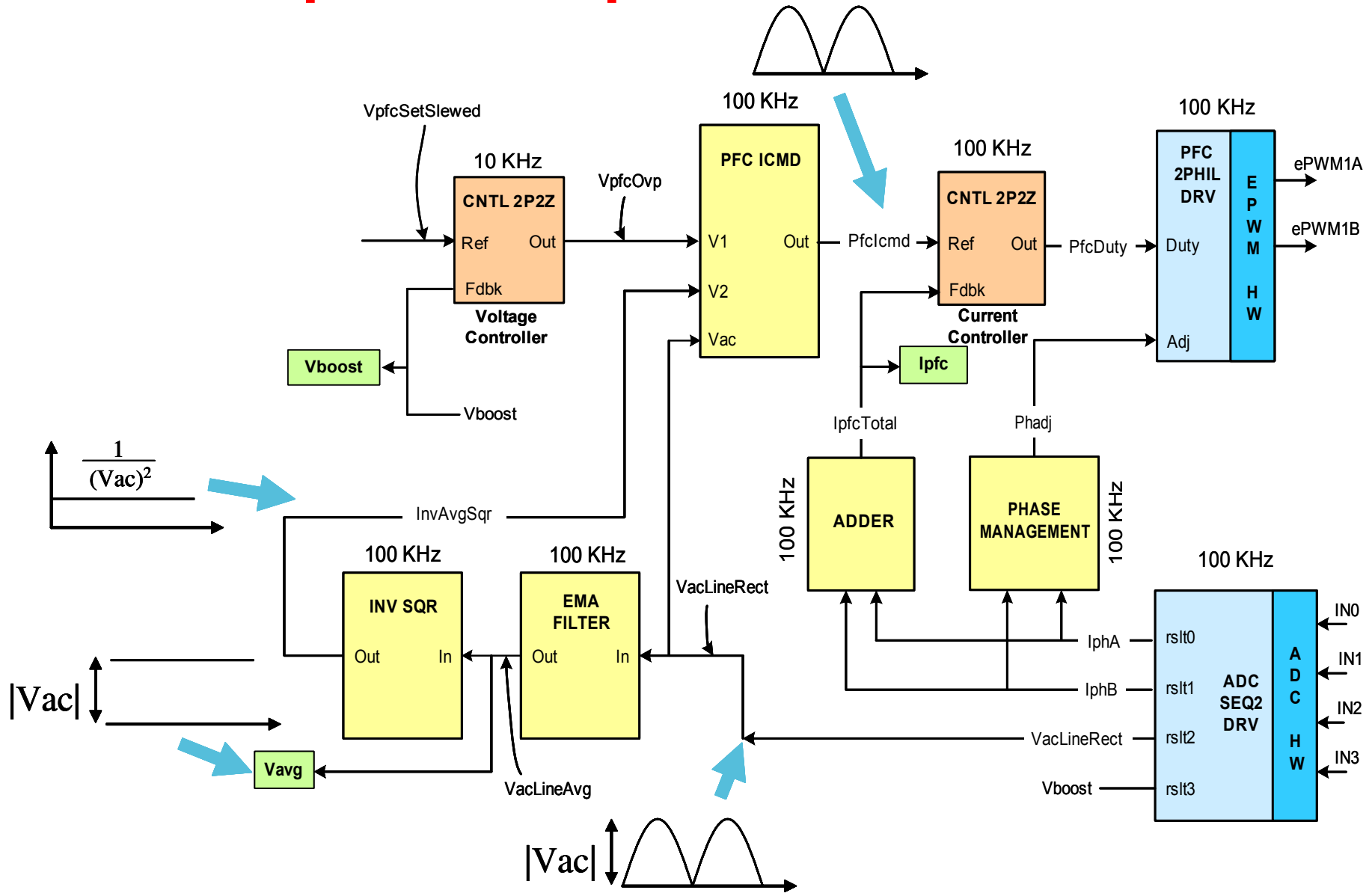
; Execute the code

```
f1
f2
f3
f4
f5
```

Peripheral Drivers



Example: Example PFC + PSFB



Agenda

- Power Systems Overview
- Why Digital Control
- Digital Controller Requirements
- Why C2000 for Digital Power
- Software Development Tools
- **Hardware Development Tools**

Piccolo controlCARD

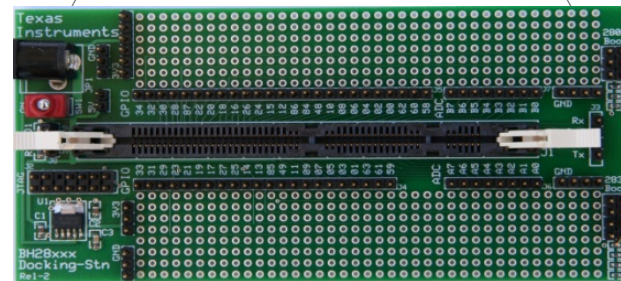
Modular, Robust, Standard

controlCARD

- **Low cost, small form factor**
- **Standard DIMM interface**
 - Includes analog I/O, digital I/O, and JTAG signals available at DIMM interface
- **Robust design**
 - Noise filter at ADC input pins
 - Ground plane
 - Isolated UART communication
 - Supply pin decoupling
- **All life support circuitry**
 - Clock, Power Supply, LDO, etc
- **Multiple versions available**
 - Piccolo F28027
 - Piccolo F28035
 - Delfino F28335
 - Delfino C28436
 - F2808
 - F28044
 - \$49-69



**Pin compatible across
the C2000 family!**



Piccolo DPS Tools Offerings

Device Evaluation



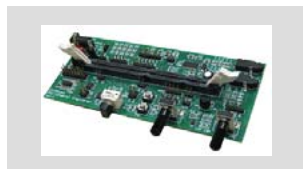
Experimenter's Kit

TMDXDOCK28027
TMDXDOCK28035
TMDSDOCK2808
TMDSDOCK28335
TMDXDOCK28343
\$79-\$159



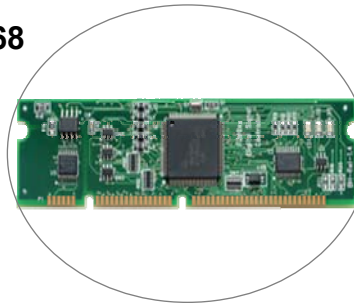
Experimenter's Kit - 168

TMDXDOCK28346-168
\$189



Peripheral Explorer

TMDSPREX28335
\$179



Application Development

Digital Power Experimenter's Kit

TMDSDCDC2KIT
\$229



Digital Power Developer's Kit

TMDSDCDC8KIT
\$325



AC/DC Developer's Kit

Interleaved 2ph PFC w/ current balancing, PSFB, Peak current mode control
TMDSACDCKIT
\$695



Resonant DC/DC Developer's Kit

LLC Resonant DC-DC
TMDSRESDCKIT
\$229



Renewable Energy Developer's Kit

TMDSENRGYKIT
\$349



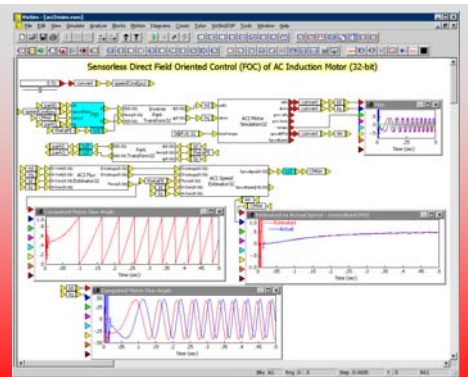
DPS Lib

Complete Library of core power control algorithms and peripheral drivers www.ti.com/controlsuite

Graphical Modeling & Code Development

VisSim and The Mathworks

- DPS and Peripheral Blocks
- Simulation and Modeling
- Auto-Tuning
- Code Generation
- Interface to CCStudio IDE
- Integration with Resonant and Renewable Energy Kits



Piccolo DPS Links

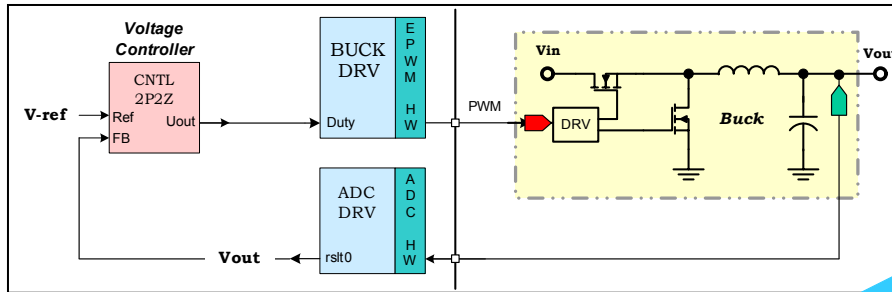
- www.ti.com/dpslib or www.ti.com/controlsuite (7/6/10)
- www.ti.com/c2000getstarted
- Using Multi-Phase DC/DC Power Supply Control
<http://training.ti.com/courses/CourseDescription.asp?iCSID=53935>
- Enabling High-Freq Power Conversion Applications
<http://training.ti.com/courses/CourseDescription.asp?iCSID=54032>
- Implementing High-BW, Low-Cycle Count Controllers
<http://training.ti.com/courses/CourseDescription.asp?iCSID=54259>
- New 4-day Workshop with new power stages and GUI configuration tool!
 - www.ti.com/biricha

Roadmap

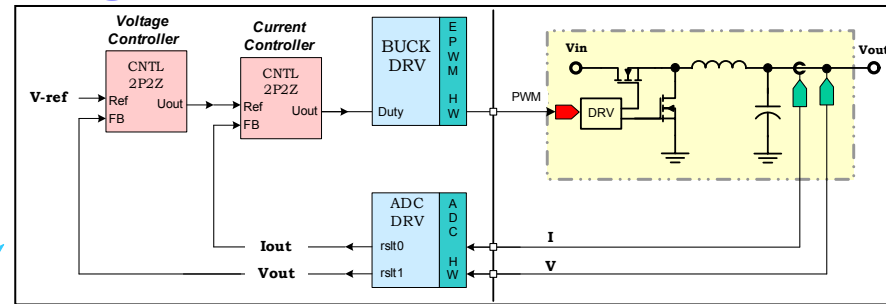
Backup

Flexible Control Methods

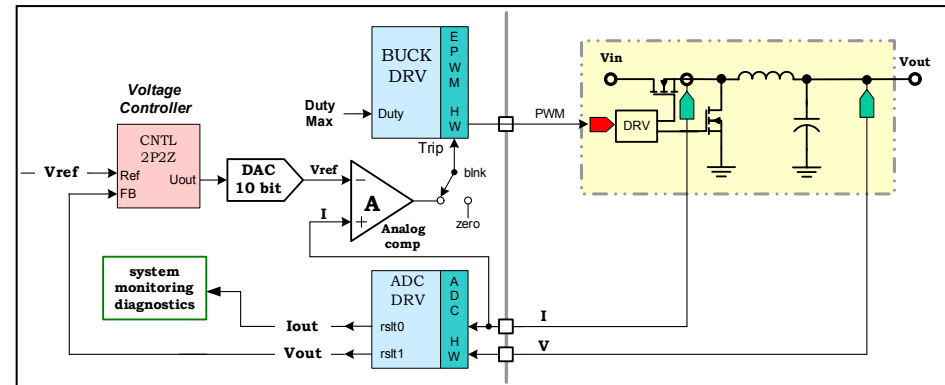
Voltage Mode



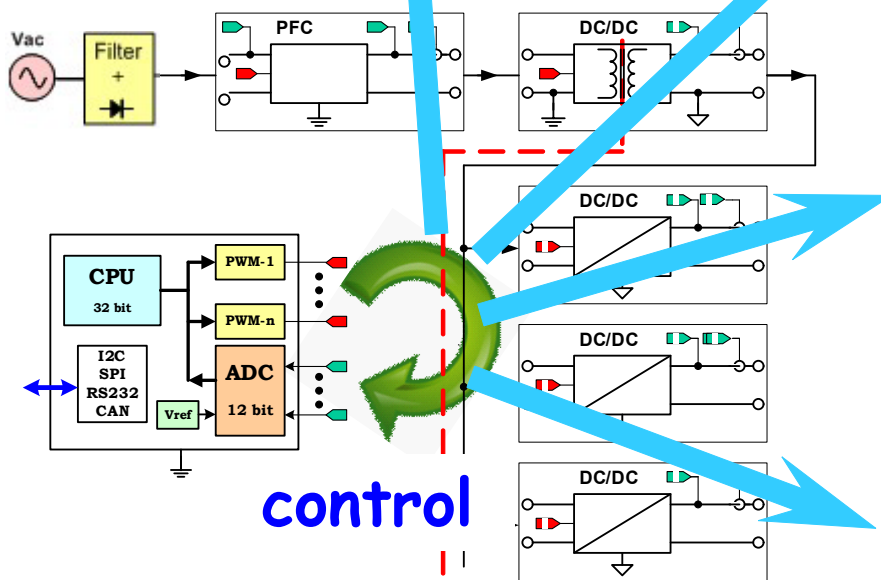
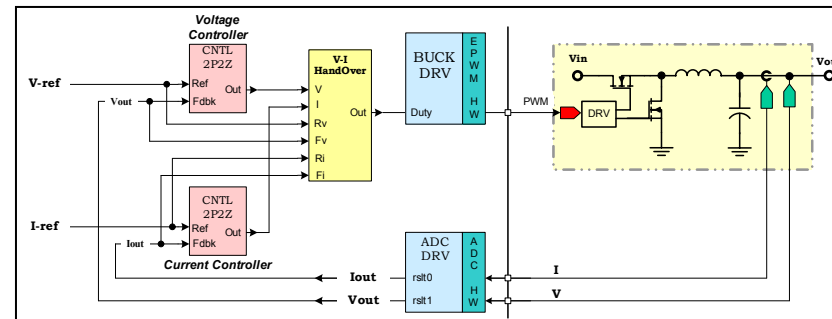
Avg Current Mode



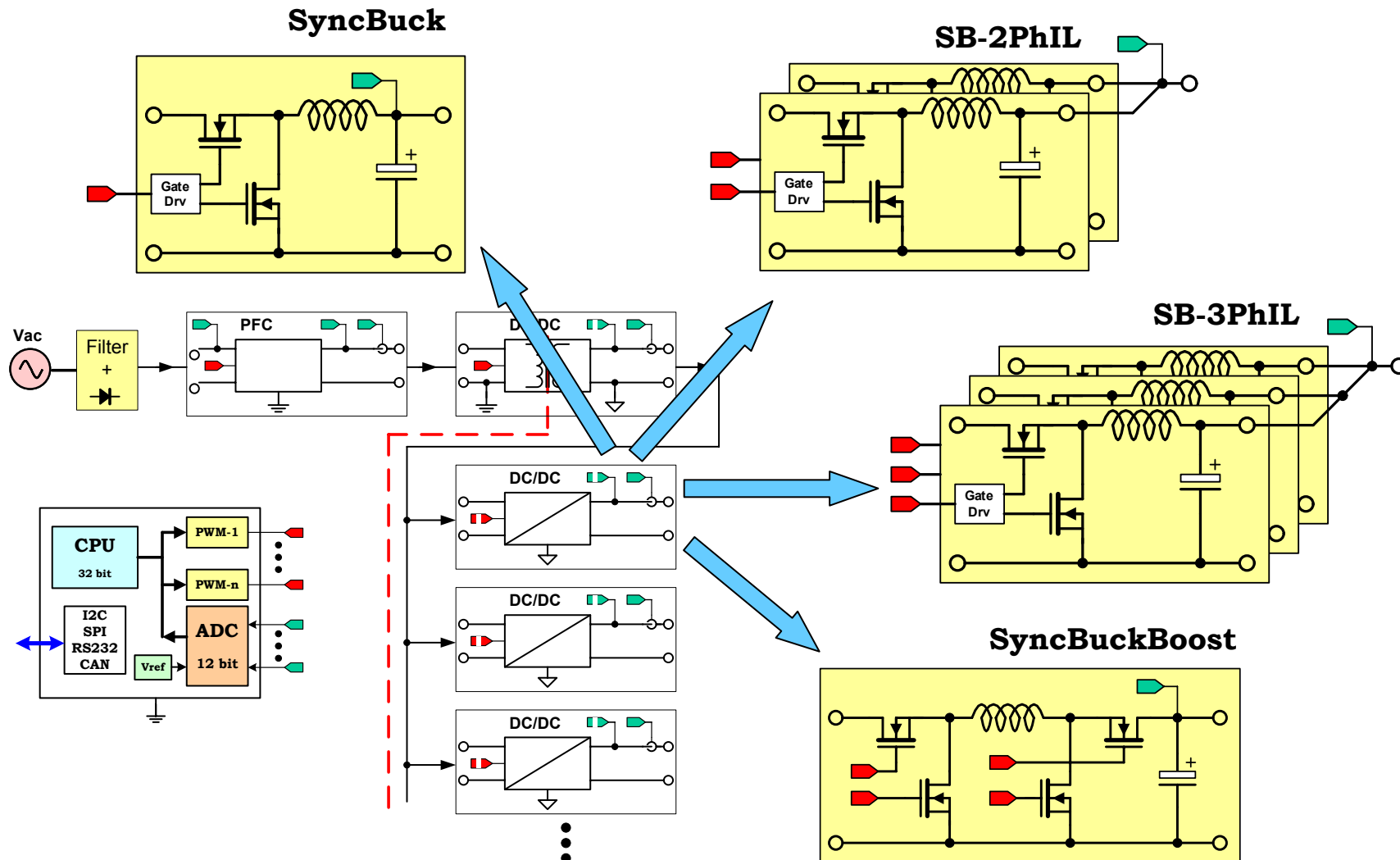
Peak / Over / CbC Current Mode



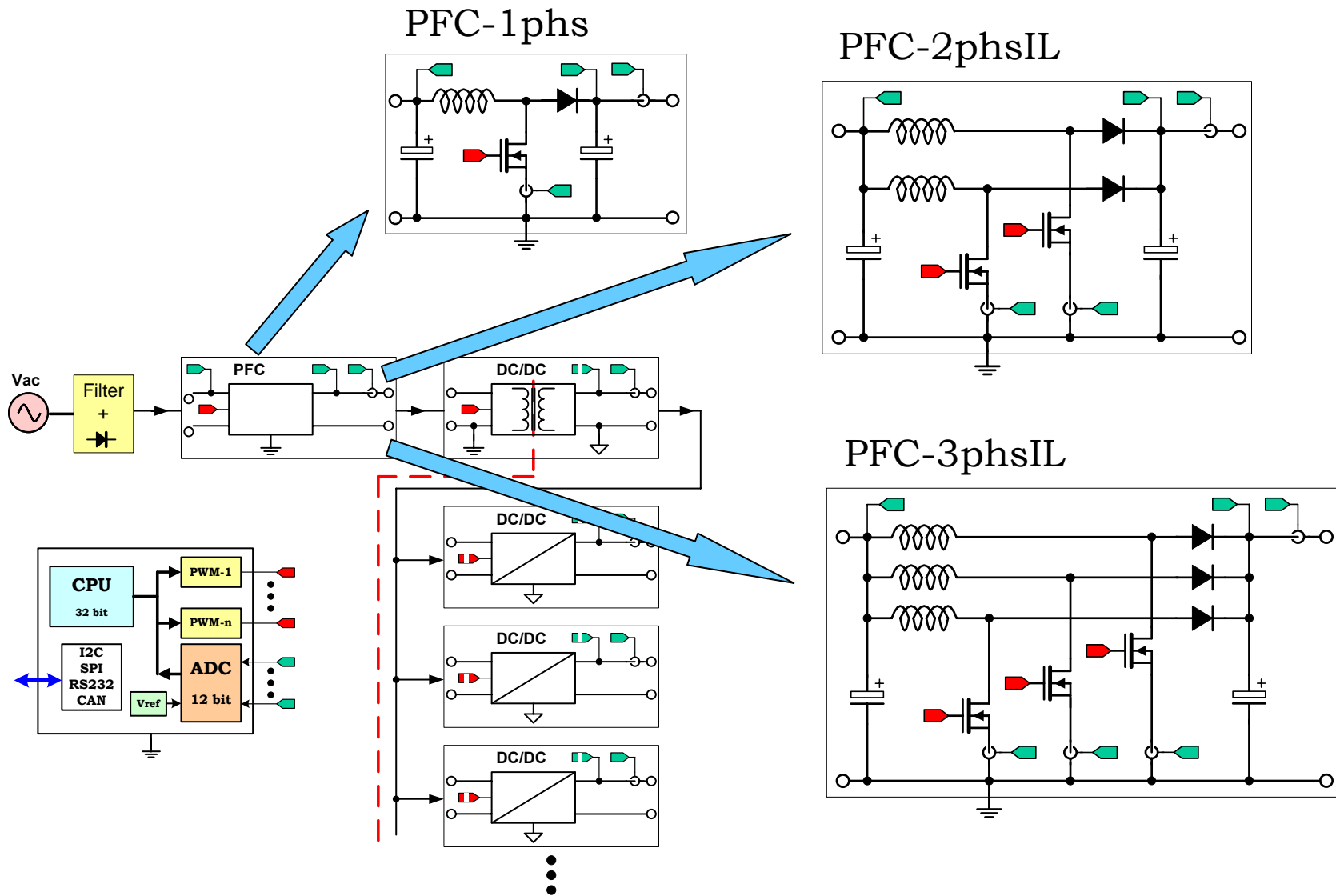
Constant Power



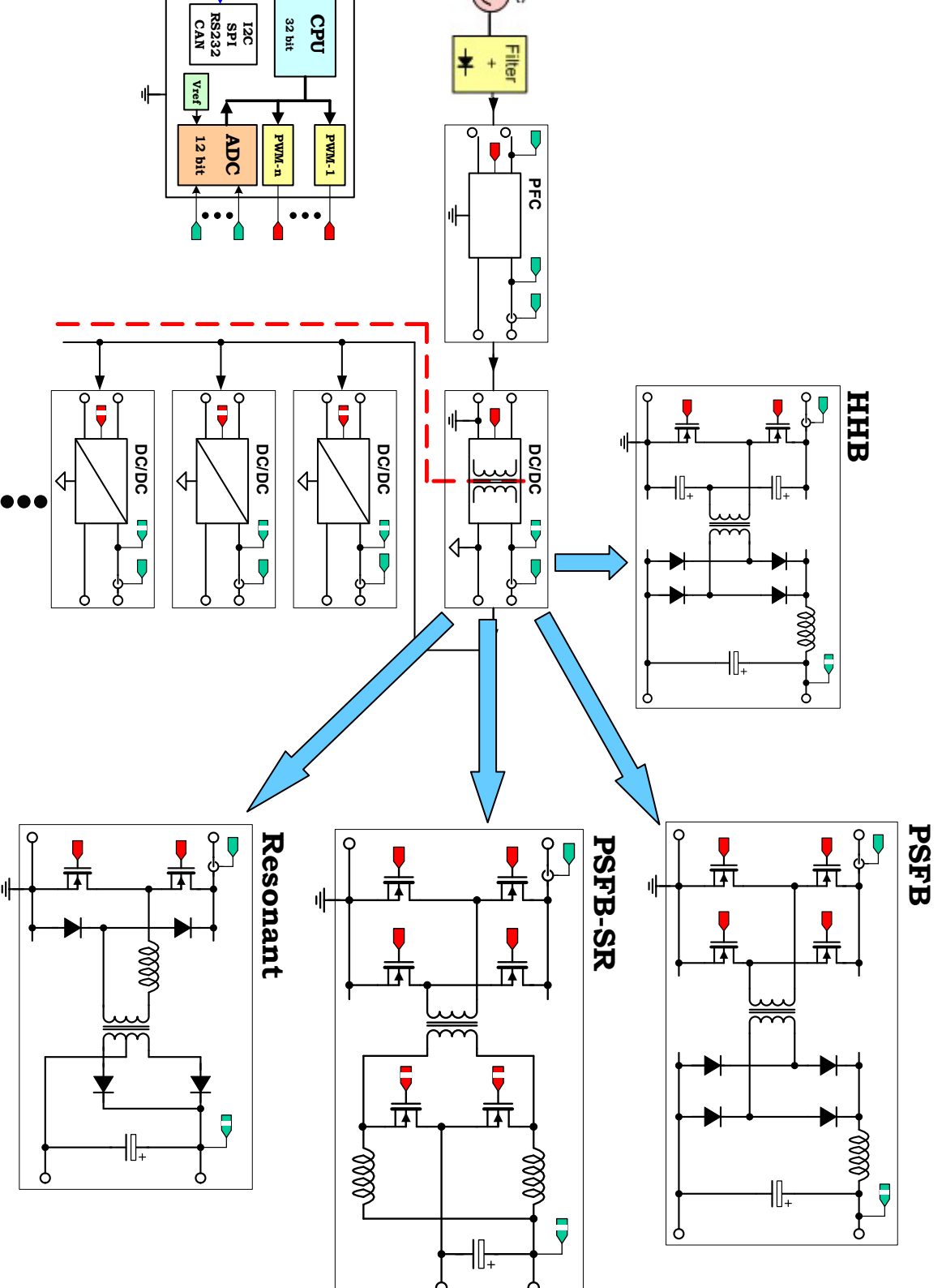
Non Isolated DC/DC Topologies



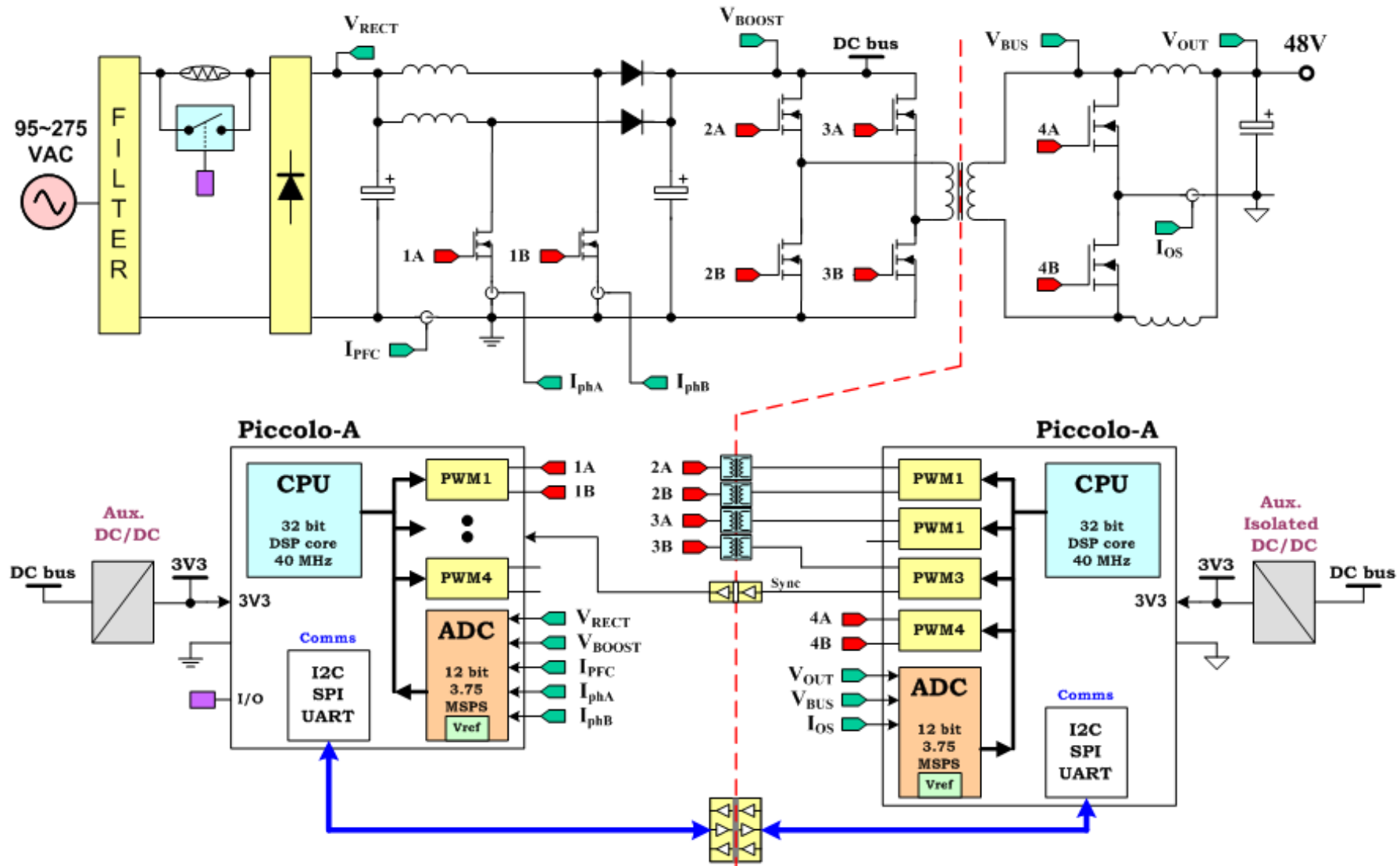
Boost/Power Factor Correction



Isolated Power Supply Topologies



Rectifier: Dual MCUs



Rectifier: Single MCU on Primary

