FAIRCHILD SEMICONDUCTOR®

February 2011

FSHDMI08 — 低电压, 宽带及带有 DDC 和 CEC 多路传输器的 HDMI 开关

特性

- 1.65MHz 非相邻通道间的串扰
- 低信号失真: 在1.65Gbps下只有-1.5dB 的衰减
- 各通道间地绝缘
- 快速启动和关闭 (< 6ns)
- 1.65Gbps 通道传输速率
- 8kV的 ESD 保护
- 低 Skew: 差分对间延迟差 <90ps,
  差分对内延迟差< 150ps
- 低功耗 (最大值为1μA)

应用

- XGA 和720p DVI 及 HDMI 视频源的选择

总述

FSHDMI08是一种宽带开关，用于发送HDMI连接信号，时钟信号及有关的DDC和CEC控制信号，对于UXGA方案，本开关的每一个通道均可支持高达1.65Gbps的数据传输速率。可以应用于包括液晶电视、DVD、机顶盒、笔记本电脑及带多路数字视频接口的其它设计中。通过FSHDMI04开关，可实现以低非邻道串扰及优质的断开隔离（Off-Isolation）性能传输HDMI信号。本性能对于减少视频应用中有效视频源之间的重影现象非常关键。本开关宽的带宽使得高速差分信号以最小的附加斜度和相位抖动通过开关。管脚输出支持HDMI标准A类连接器在PCB上的设计。

重要提示:

欲知其它详情，请 analogswitch@fairchildsemi.com.

订购信息

订购编号	Eco Status	封装说明	Package Description
FSHDMI08MTDX	RoHS	56-引脚，超薄小封装 (TSSOP), JEDEC MO-153, 6.1mm 宽	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

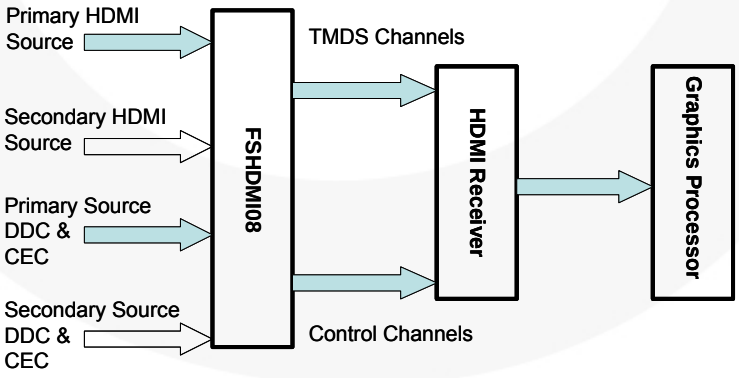


图 1. 单一连接 HDMI 应用

功能图

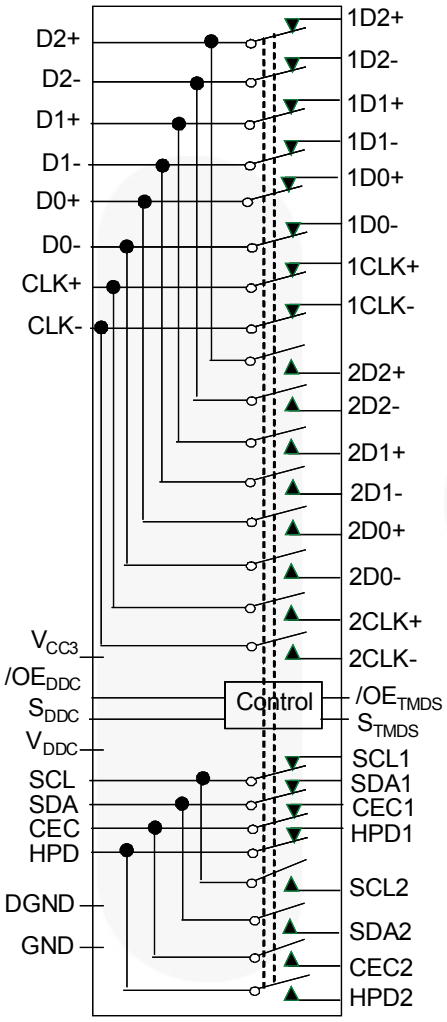


图 2.　功能图

管脚描述

管脚 #	名称	描述
1-4,6,7,11-14,16,17, 47,48,50,51,53,54	1Dn+, 1Dn-, 2Dn+, 2Dn-, Dn+, Dn-	TMDS 数据通道
8,9,18,19,44,45	1CLK+, 1CLK-, 2CLK+, 2CLK-, CLK+, CLK-	TMDS 时钟通道
24,28,33	HPD1, HPD2, HPD	热插入侦测
22,26,35	SCL1, SCL2, SCL	显示时钟通道 (DDC)
23,27,34	SDA1, SDA2, SDA	显示数据通道 (DDC)
21,25,36	CEC1, CEC2, CEC	消费电子控制 (CEC)
29	V_{DDC}	DDC 供电
20,39,40,55,56	V_{CC3}	TMDS 供电
30	DGND	DDC/CEC 接地
5,10,15,38,43,46,49,52	GND	大地
32,42	S_{TMDS}, S_{DDC}	选择管脚 (TMDS, DDC)
31,41	$/OE_{TMDS}$, $/OE_{DDC}$	输出使能 (TMDS, DDC)

管脚分配

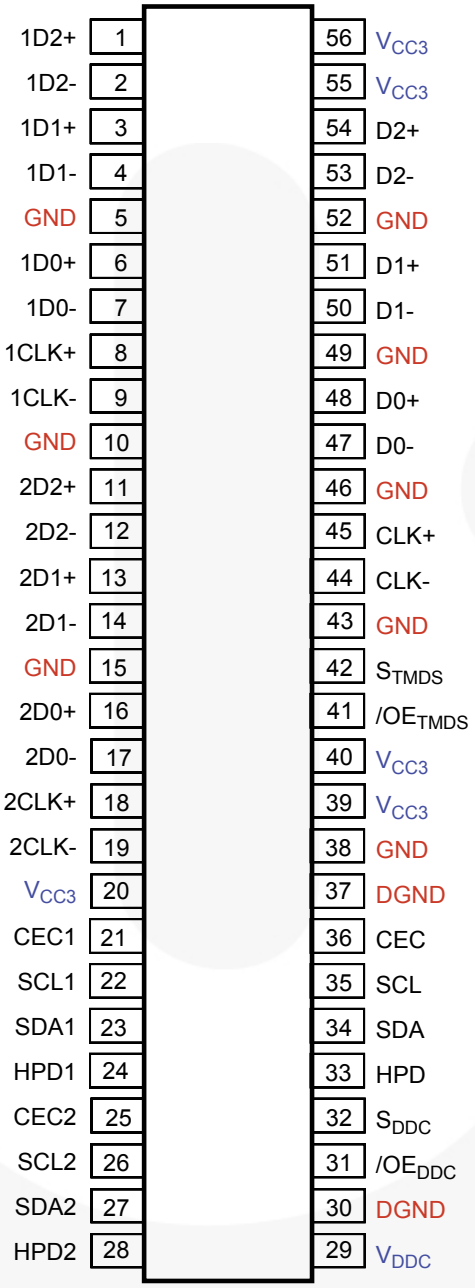


图 3. 管脚

分配图

S_{TMDS},S_{DDC}	$/OE_{TMDS}$, / OE_{DDC}	功能
Don't' Care	Logic Level HIGH	所有端口断开 (Hi-Z)
Logic Level LOW	Logic Level LOW	1Dn+/1Dn-=Dn+/Dn-; 1CLK+/ 1CLK-=CLK+/CLK-; HPD1=HPD; SCL1=SCL; SDA1=SDA; CEC1=CEC
Logic Level HIGH	Logic Level LOW	2Dn+/2Dn-=Dn+/Dn-; 2CLK+/ 2CLK-=CLK+/CLK-; HPD2=HPD; SCL2=SCL; SDA2=SDA; CEC2=CEC

绝对最大值

超出绝对最大额定值会破坏设备 ,设备会不工作或者说不建议设备在和超过建议的工作条件下被操作。
另外, 过长的暴露在超过建议工作条件下会影响设备的可靠性。这种绝对最大额定值仅仅是极端额定值。

表达符号	参数		最小值	最大值	单位
V_{CC3}	供电电源 – TMDS 通道		-0.5	4.6	V
V_{DDC}	供电电源 – 5V DDC		-0.5	6.0	V
V_{SWTMDS} (1)	开关输出/输入电压	1Dn+, 1Dn-, 2Dn+, 2Dn-, Dn+, Dn-, 1CLK+, 1CLK-, 2CLK+, 2CLK-, CLK+, CLK-	-0.5	V_{CC3} + 0.3	V
V_{SWDDC} (1)	开关输入/输出电压	HPD1, HPD2, HPD, SCL1, SCL2, SCL, SDA1, SDA2, SDA, CEC1, CEC2, CEC	-0.5	V_{DDC} + 0.3	V
V_{CNTRLT} (1)	控制输入电压	S_{TMDS}, /OE_{TMDS}	-0.5	4.6	V
V_{CNTRLD} (1)	控制输入电压	S_{DDC}, /OE_{DDC}	-0.5	6.0	V
I_{IK}	输入钳位二极管电流			-50	mA
I_{SW}	开关输入/出电流 (续)			128	mA
T_{STG}	储存温度范围		-65	+150	°C
T_J	最高结点温度			+150	°C
T_L	导线温度(焊接, 10秒)			+260	°C
ESD	人体电流模式 (JEDEC: JESD22-A114)	I/O接地		8.0	kV
		所有管脚		2.5	
	人体电流模式 (JEDEC: JESD22-C101)			2.0	kV

注解

1. 如输入及输出二极管电流额定值均达到时则可能会超出输入及输出负额定值。

推荐工作条件

推荐工作条件表中定义的是实际元件工作的条件。推荐工作条件指定用于保证实现数据表规范的最佳性能， Fairchild 建议不得超出以上值或设计至最大绝对额定值.

表达符号	参数	最小值	最大值	单位
V_{CC3}	TMDS 供电电压 – 3V	3.0	4.3	V
V_{DDC}	DDC 供电电压	3.0	5.5	V
V_{CNTRLT}	控制输入电压 – S_{TMDS}, /OE_{TMDS}	0	V_{CC3}	V
V_{CNTRLD}	控制输入电压 – S_{DDC}, /OE_{DDC}	0	V_{DDC}	V
V_{SWTMDS}	开关输入/出电压对于 HDM I路径	V_{CC3} – 0.6	V_{CC3}	V
V_{SWDDC}	开关输入/出电压对于 DDC 路径	0	V_{DDC}	V
T_A	工作温度	-40	85	ºC
θ_{JA}	热阻 (大气)		80	ºC/W

DC电气特性

如无其它规定，均为在 25°C 下 V_{CC3}=3.3V, V_{DDC}=5.0V 的典型值.

表达符号	参数	V_{CC3} / V_{DDC} (V)	条件	T_A=- 40°C 至 +85°C			单位
				最小	典型	最大	
V_{IK}	钳位二极管电压	V_{CC3}=3.0 V_{DDC}=5.0	I_{IN}=-18mA			-1.2	V
V_{IH}	控制输入电压高平	V_{CC3}=3.0 至 3.6 V_{DDC}=3.0 至 5.5		2			
V_{IL}	控制输入电压低平	V_{CC3}=3.0 至 3.6 V_{DDC}=3.0 至 5.5				0.8	V
I_{OZTMDS}	断开状态漏电流 TMDS 通道	V_{CC3}=3.6 V_{DDC}=5.5	0 ≤ V_{SWTMDS} ≤ V_{CC3} 图 5	-1		1	µA
I_{OZDDC}	断开状态漏电流 DDC/CEC 通道	V_{CC3}=3.6 V_{DDC}=5.5	0 ≤ V_{SWDDC} ≤ V_{DDC} 图 5	-5		5	µA
I_{INTMDS}	控制输入漏电流 (S_{TMDS}, /OE_{TMDS})	V_{CC3}=3.6 V_{DDC}=5.5	V_{SWDDC}=0 to V_{CC3}	-1		1	µA
I_{INDDC}	控制输入漏电流 (S_{DDC}, /OE_{DDC})	V_{CC3}=3.6 V_{DDC}=5.5	V_{SWDDC}=0 to V_{DDC}	-1		1	µA
I_{CC3}	静态供电电流 - TMDS	V_{CC3}=3.6 V_{DDC}=5.5	V_{SWTMDS}=V_{CC3} – 0.6 or V_{CC3}, I_{OUT}=0			2	µA
I_{DDC}	静态供电电流 - DDC	V_{CC3}=3.6 V_{DDC}=5.5	V_{SWDDC}=0 或 V_{DDC}, I_{OUT}=0			2	µA
ΔI_{CCT3}	I_{CC3}的增值	V_{CC3}=3.6 V_{CC5}=5.5	一端输入3.0V; 其它输入在 V_{CC3}-0.6 或 V_{CC3}			100	µA
ΔI_{CCTD}	I_{DDC}的增值	V_{CC3}=3.6 V_{CC5}=5.5	一端输入3.0V; 其它输入在 V_{DDC}			15	µA

AC电气特性

如无其它规定，均为在 25°C 下 V_{CC3}=3.3V, V_{DDC}=5.0V 的典型值.

表达符号	参数	V_{CC3} / V_{DDC} (V)	条件	T_A=- 40ºC 至 +85ºC			单位
				最小	典型	最大	
TMDS通道							
t_{ONTMDS}	打开时间 S, /OE 到输出	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	V_{SWTMDS}=V_{CC3} -0.5, R_{PU}=50Ω, C_L=5pf 图 6, 图 7		4	6	ns
$t_{OFFTMDS}$	关闭时间 S 到输出	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	V_{SWTMDS}=V_{CC3} -0.5, R_{PU}=50Ω, C_L=5pf 图 6,图 7		2	4	
$t_{BBM-TMDS}$	先断后通时间(2)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	V_{SWTMDS}=V_{CC3} -0.5, R_{PU}=50Ω, C_L=5pf 图 15	1			ns
t_{pd} (t_{pLH},t_{pHL})	开关传输延迟(2)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	R_{PU}=50Ω, C_L=5pf 图 14			4000	ps
t_{jitter}	总抖动 (DJ+RJ)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	f=165MHz clock with 50% duty cycle, R_{PU}=50Ω, C_L=5pf 图 14			90	ps
t_{ratio}	占空比	V_{CC3}=3.0 至 3.6 V_{DDC} =5.0	f=165MHz clock with 50% duty cycle, R_{PU}=50Ω, C_L=5pf 图 14	40	50	60	%
t_{SK1}	差分对间延迟差 (TMDS Cn+ 至 Cn-)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	f=1.65Gbps, 2^{23}-1 PRBS, R_{PU}=50Ω, C_L=5p图 14		55	100	ps
t_{SK2}	差分对内延迟差 (任意两个TMDS 开关通道之间)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	f=1.65Gbps, 2^{23}-1 PRBS, R_{PU}=50Ω, C_L=5pf 图 14		90	160	ps
$OIRR_{TMDS}$	隔离度 (TMDS通道)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	R_T=50Ω, f=370MHz 图 10	-30			dB
		V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	R_T=50Ω, f=825MHz 图 10	-25			
$Xtalk_{TMDS}$	非相邻通道串扰 (TMDS通道)	V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	R_T=50Ω, f=370MHz 图 11	-25			dB
		V_{CC3}=3.0 至 3.6 V_{DDC}=5.0	R_T=50Ω, f=825MHz 图 11	-20			
f_{max}	最大数据波特(2)	V_{CC3}=3.3 V_{DDC}=5.0			1.65		Gbps
控制通道 – DDC / CEC							
t_{ONDDC}	打开时间; S_{DDC}, $/OE_{DDC}$到输出	V_{CC3}=3.3 V_{DDC}=3.0 至 5.5	V_{SWDDC}=2V, R_{DDC}=1kΩ, C_L=5pf			28	ns
t_{OFFDDC}	关闭时间; S_{DDC}, $/OE_{DDC}$ 到输出	V_{CC3}=3.3 V_{DDC}=3.0 至 5.5	V_{SWDDC}=2V, R_L=1kΩ, C_L=5pf			24	ns

注:

2. 以上参数由特性和设计保证.

测试图

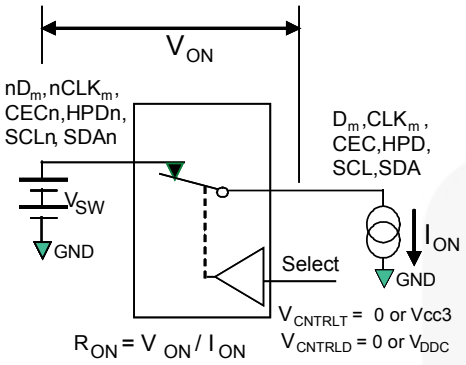
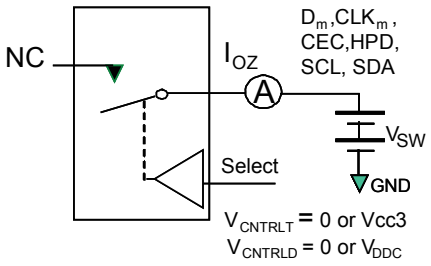
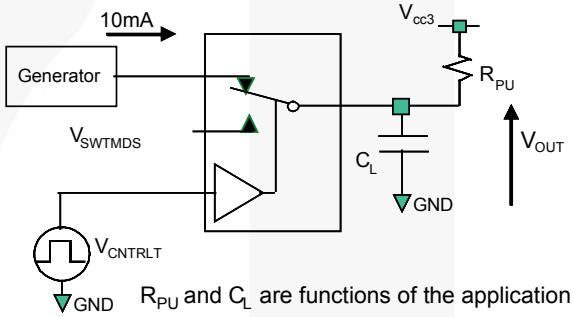


图 4. 导通电阻



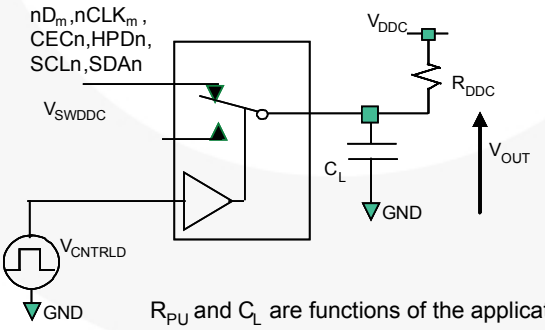
Each switch port is tested separately.

图 5. 断开漏电流



R_{PU} and C_L are functions of the application environment (see AC/DC tables for values of C_L and R_{PU}).
C_L includes test fixture and stray capacitance.

图 6. TMDS测试电路负载



R_{PU} and C_L are functions of the application environment (see AC/DC tables for values of C_L and R_{DDC}).
C_L includes test fixture and stray capacitance.

图 7. DDC 测试电路负载

测试图

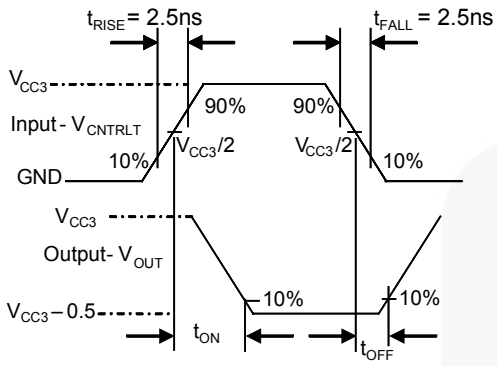


图 8.　打开 / 关闭波形

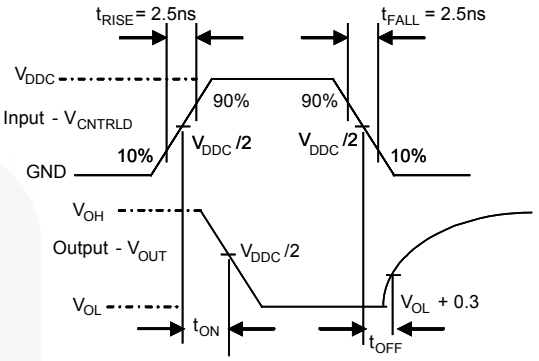


图 9.　DDC打开 / 关闭波形

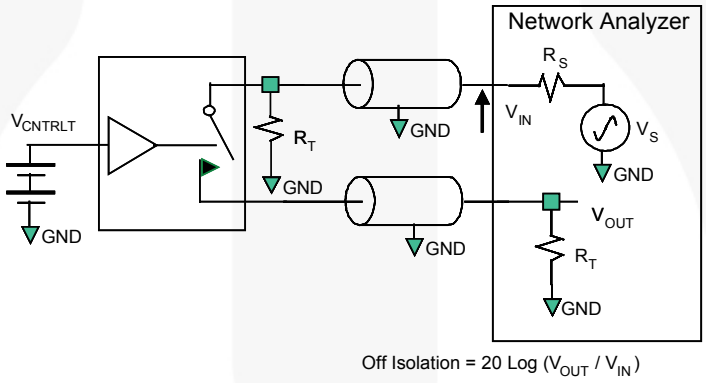


图 10.　通道隔离度

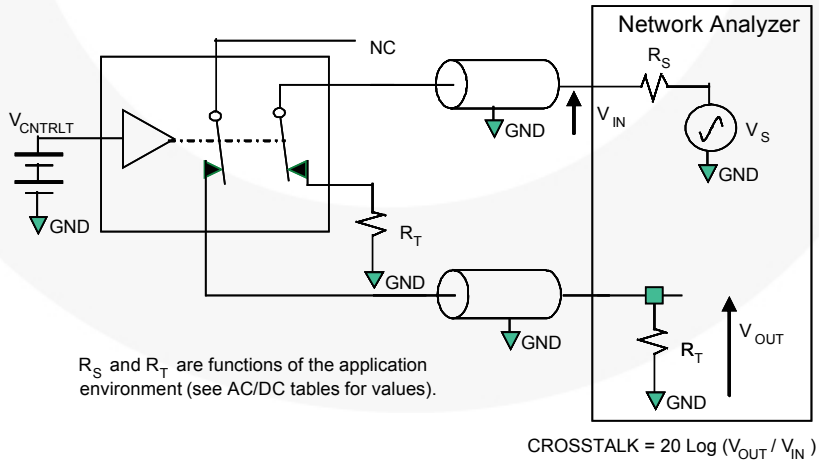


图 11.　非相邻通道间的串扰

测试图

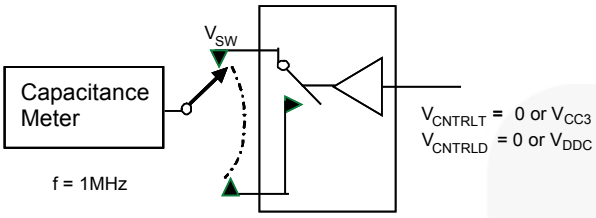


图 12. 通道断开电容

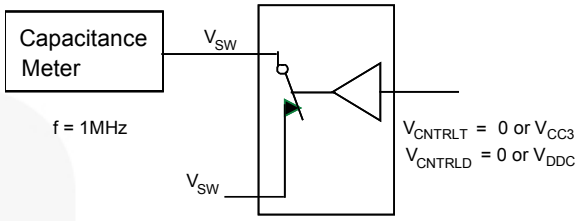


图 13. 通道导通电容

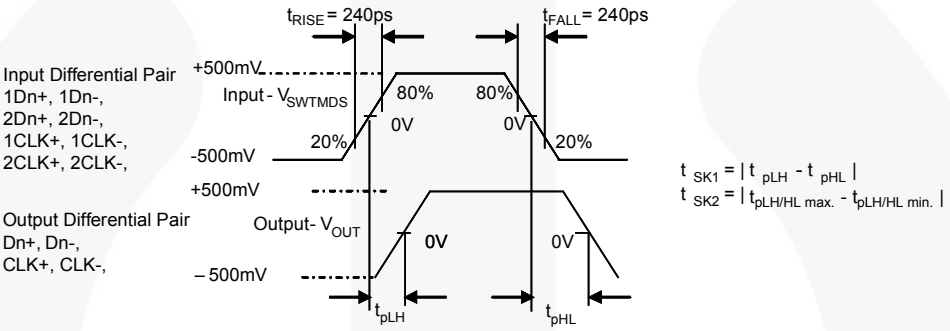
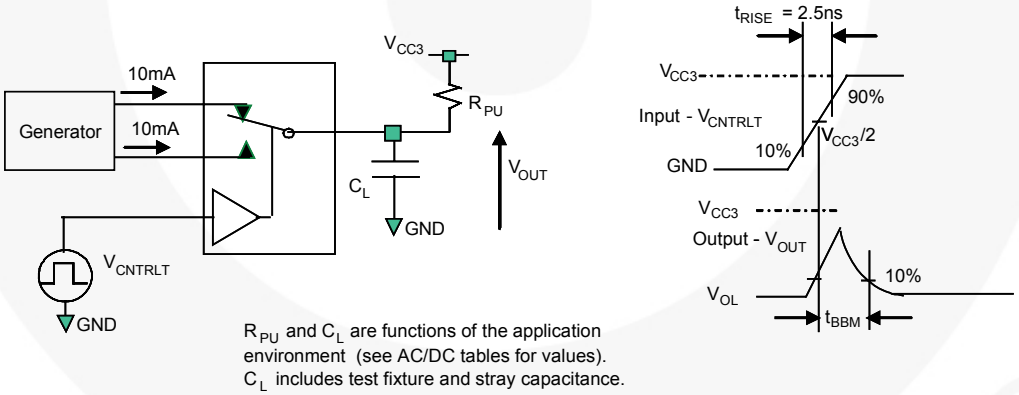


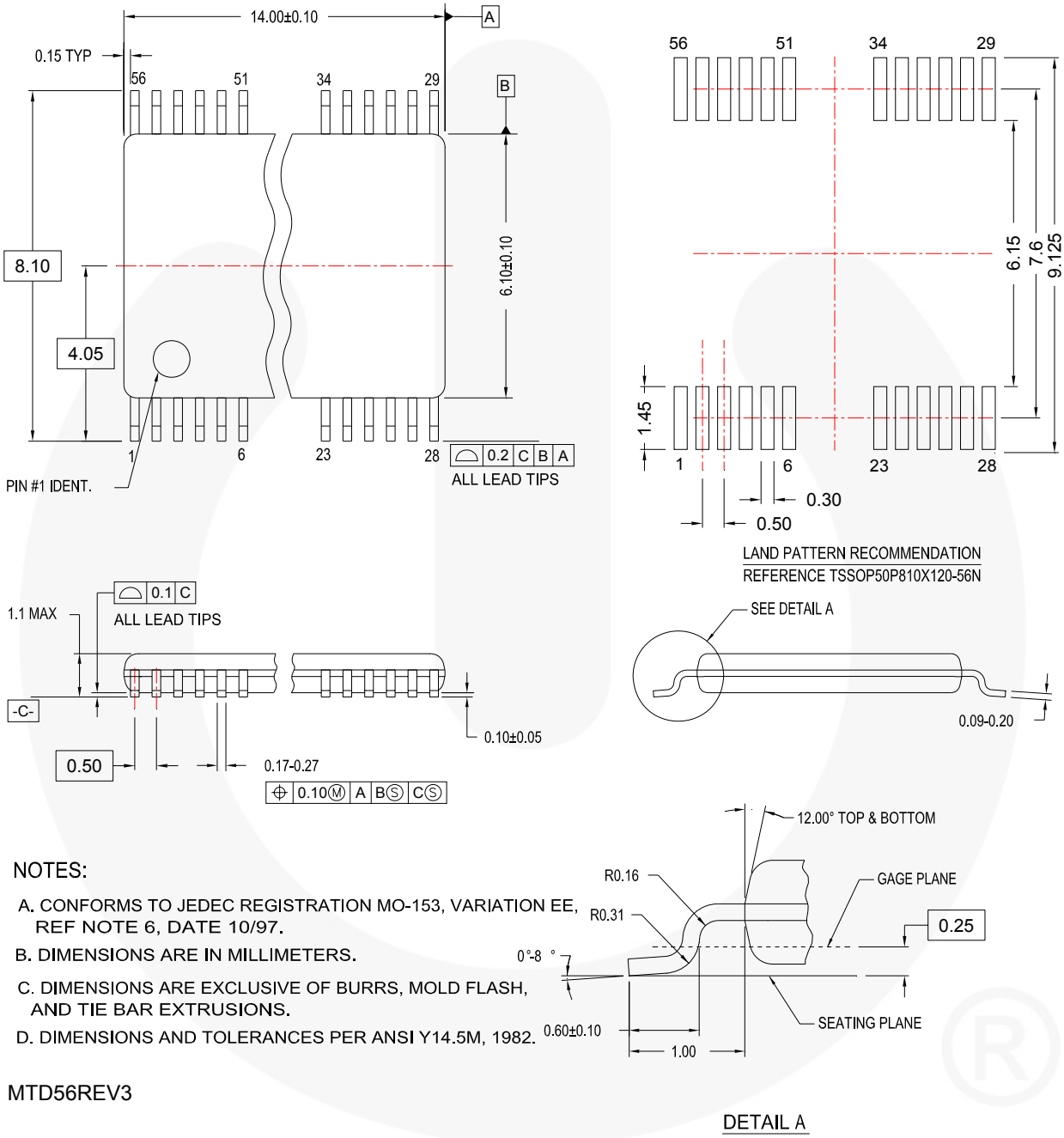
图 14. 差分对间和对内延迟差Tpd



R_{PU} and C_L are functions of the application environment (see AC/DC tables for values).
C_L includes test fixture and stray capacitance.

图 15. 先断后开

物理尺寸



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EE, REF NOTE 6, DATE 10/97.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD56REV3

图 16. 56-引脚，超薄小封装 (TSSOP)

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Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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