STM32 PMSM SDK 5.2 training

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Peripherals for advanced motor control Overview

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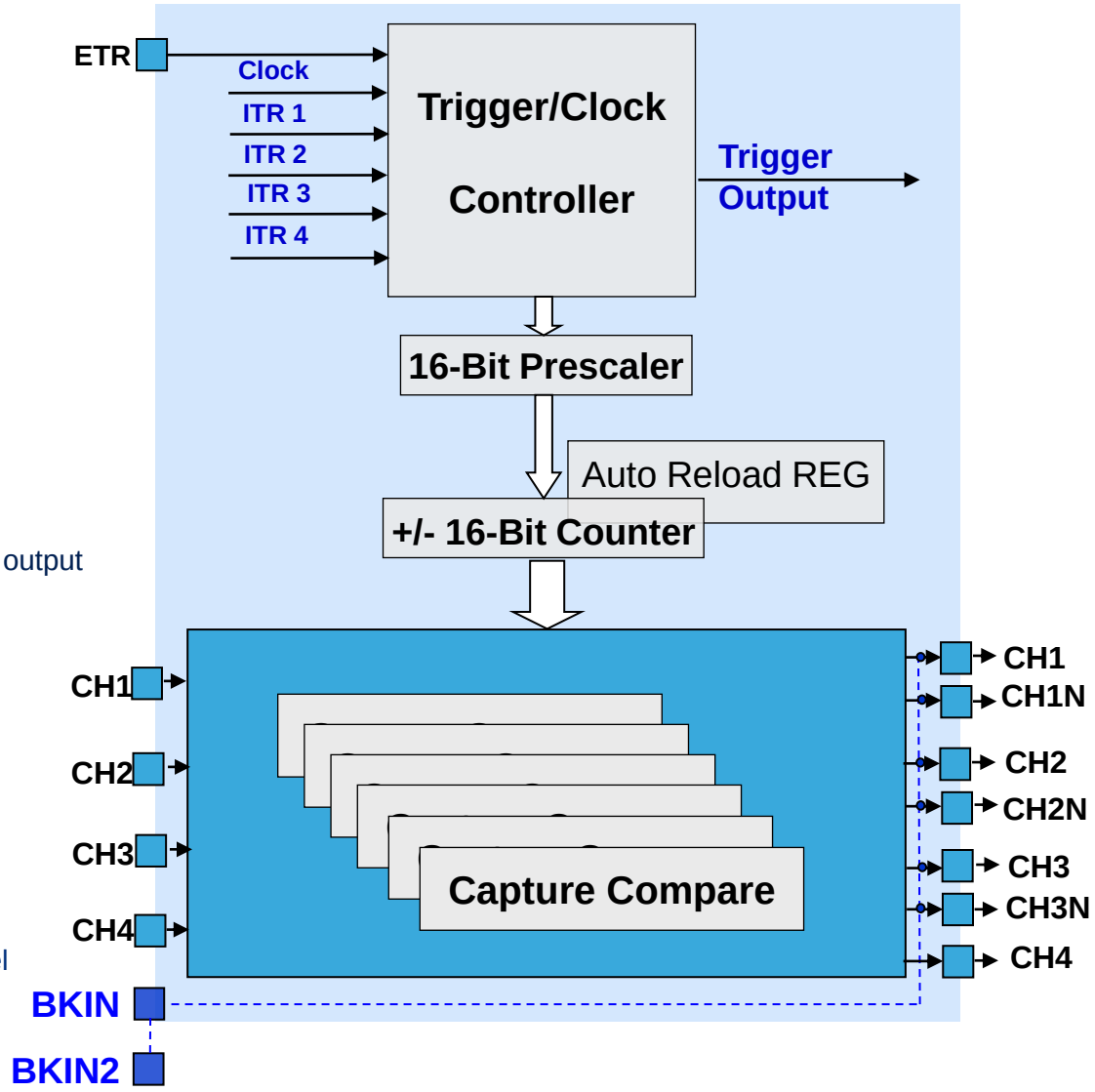
Peripherals for advanced motor control

- **PWM generation**
- Speed / position feedback
- Multi timer configuration
- Analog to Digital converter
- Other inbuilt peripherals (DMA, connectivity)

Advanced timer Features overview

- TIM1, 8 (,20) on High Speed APB (APB2)
- Internal clock up to 144 MHz
- 16-bit Counter
- Up, down and centered counting modes
- Auto Reload
- 4 (6) x 16-bit Capture Channels
- Output Compare
- PWM
- Input Capture, PWM input Capture
- One Pulse Mode
- 6 Complementary outputs: Channel1, 2 and 3
- Output Idle state selection independent for each output
- Polarity selection independent for each output
- Programmable PWM repetition counter
- Hall sensor interface
- Encoder interface
- 8 Independent IRQ/DMA Requests Generation
- Embedded Safety features
- Break inputs
- Lockable unit configuration: 3 possible Lock level



PWM Mode

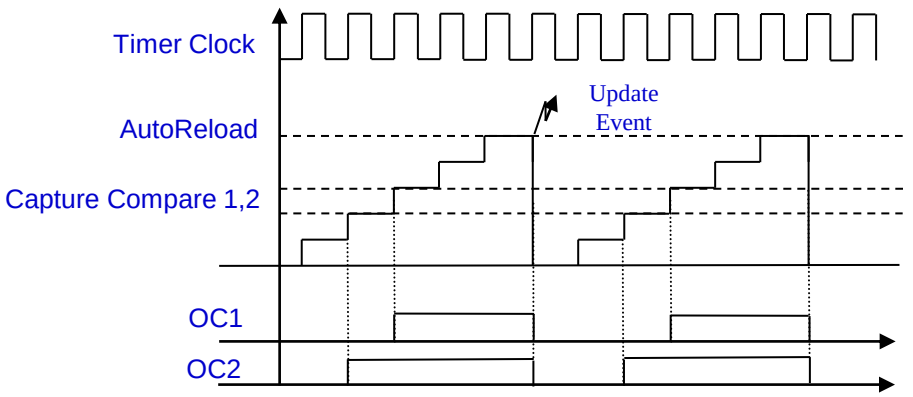
- The PWM mode allows to generate:
- 7 independent signals for TIM1 and TIM8 (TIM20)
- 4 independent signals for TIM2, 3 and 4
- Max input clock is 72MHz to provide 13.8ns edge resolution (12-bit @16kHz edge-aligned PWM)
- The frequency and a duty cycle determined as follow:
- One auto-reload register to defined the PWM period.
- Each PWM channel has a Capture Compare register to define the duty cycle.

➔ Example: to generate a 40 KHz PWM signal w/ duty cycle of 50% on TIM1 clock at 72MHz:

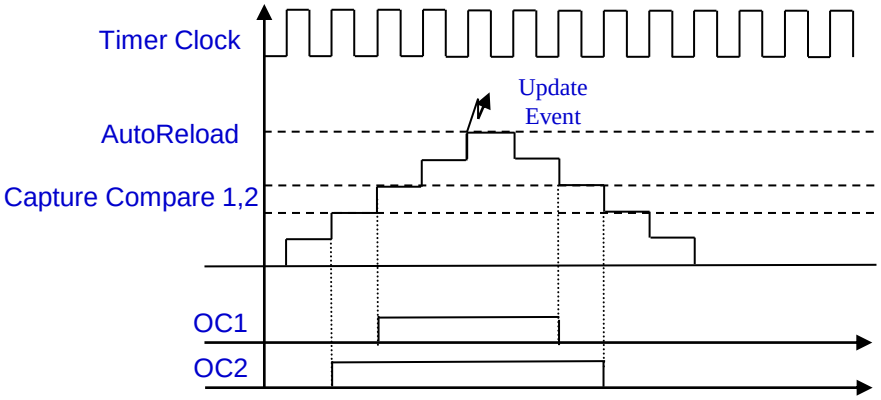
- Load Prescaler register with 0 (counter clocked by TIM1CLK/(0+1)), Auto Reload register with 1799 and CCRx register with 899

- There are two configurable PWM modes:

Edge-aligned Mode

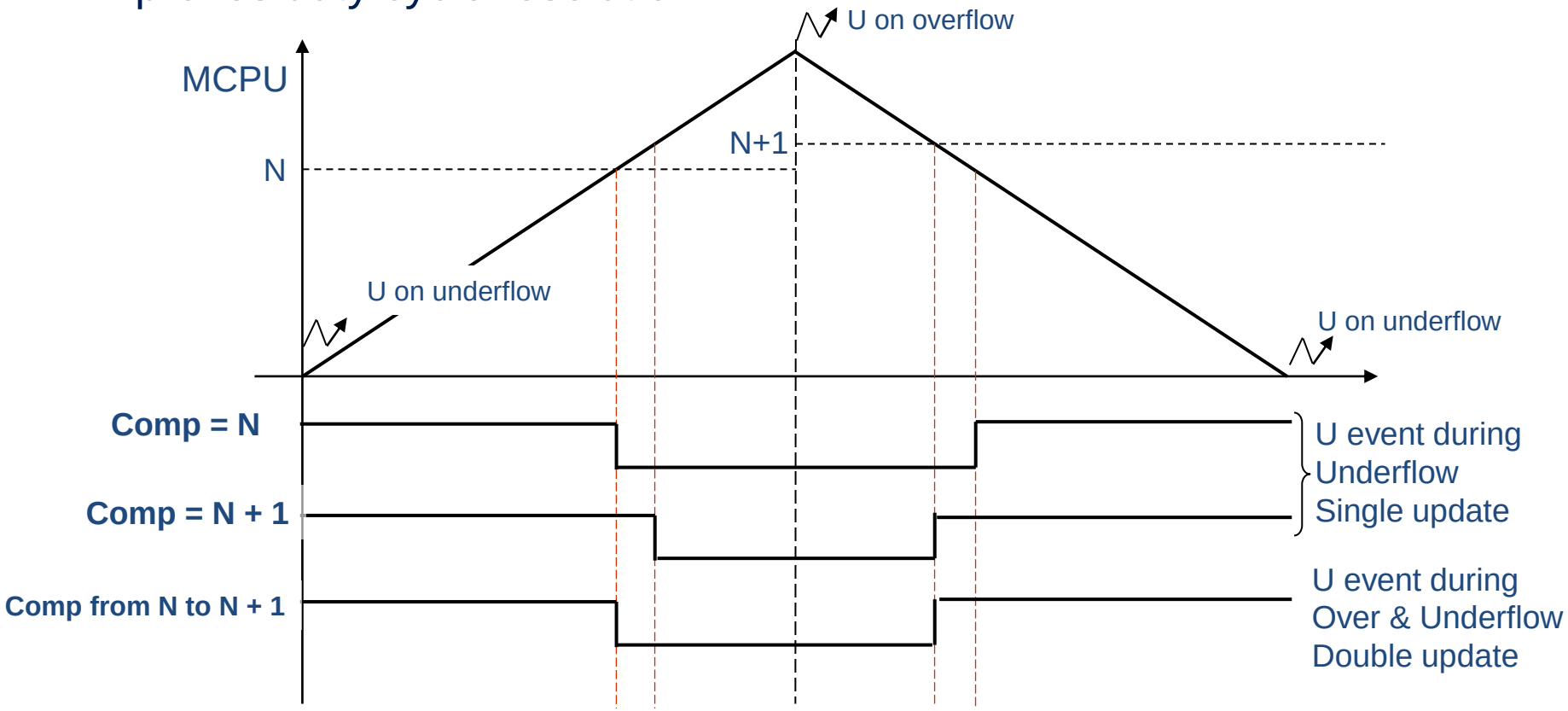


Center-aligned Mode



Double Update Mode

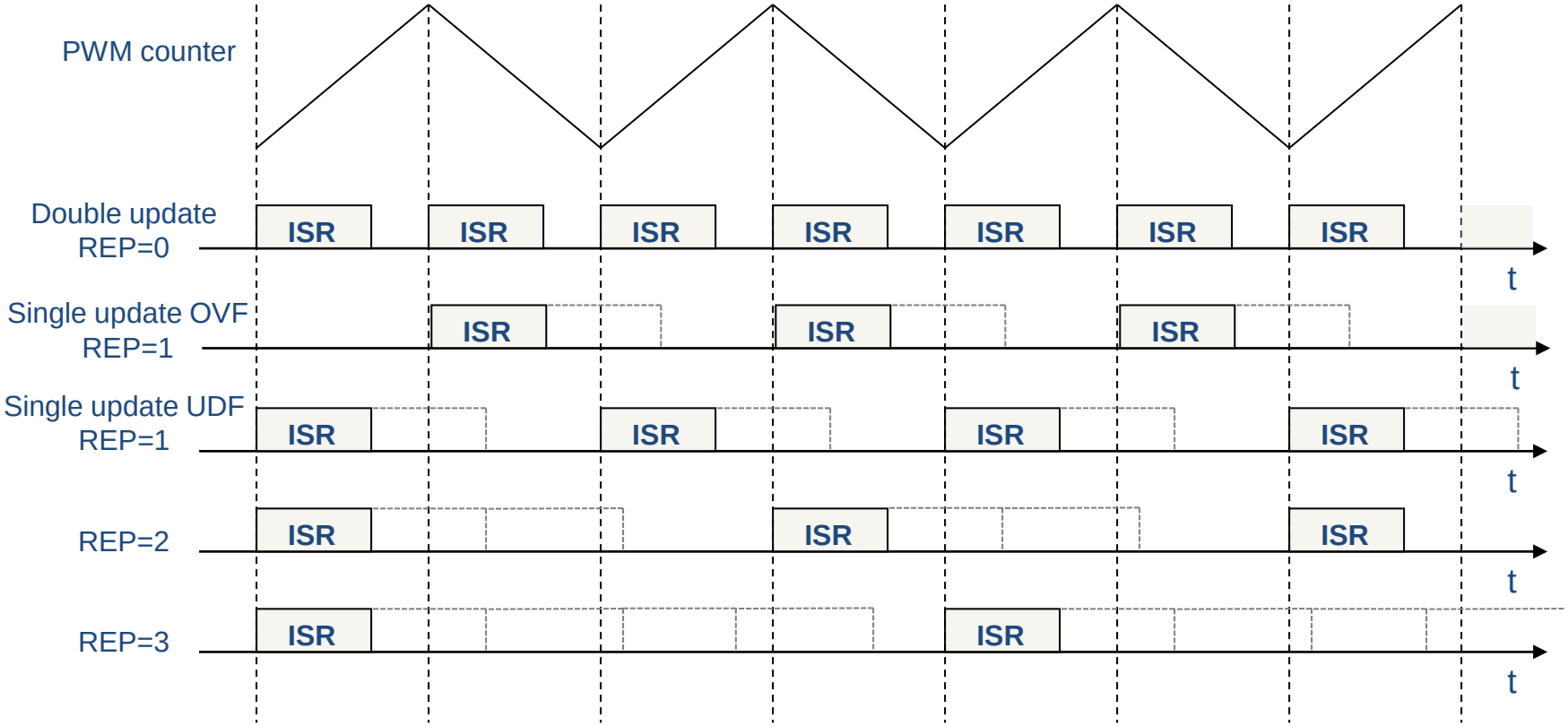
- An Update event (U) during the Overflow of the PWM counter improves duty cycle resolution.



PWM main Interrupt Service Routine

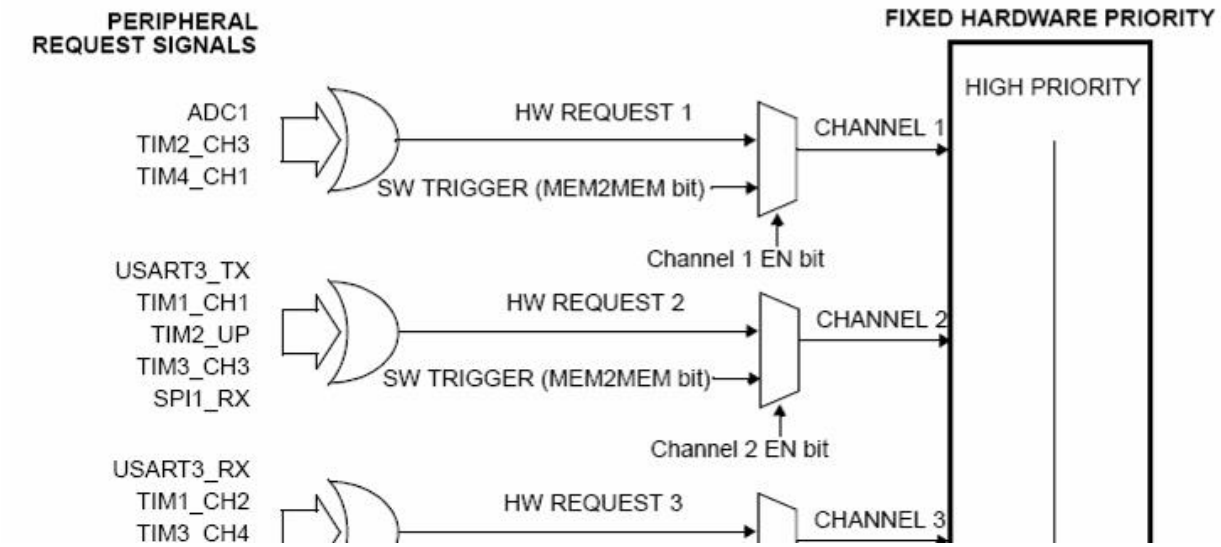
- So-called U (Update) event
  - Synchronously transfers all preload into active registers
    - 3 (4) compares for duty cycles
      - Preload mechanism can be disabled if needed
    - 1 Auto Reload for PWM switching period
      - allows changing on-the-fly the PWM frequency while maintaining duty cycles
    - PWM clock prescaler
- Adjustable U event rate
  - programmable through a 8-bit repetition counter
  - Allows to choose Overflow/Underflow or both for update

Repetition Counter



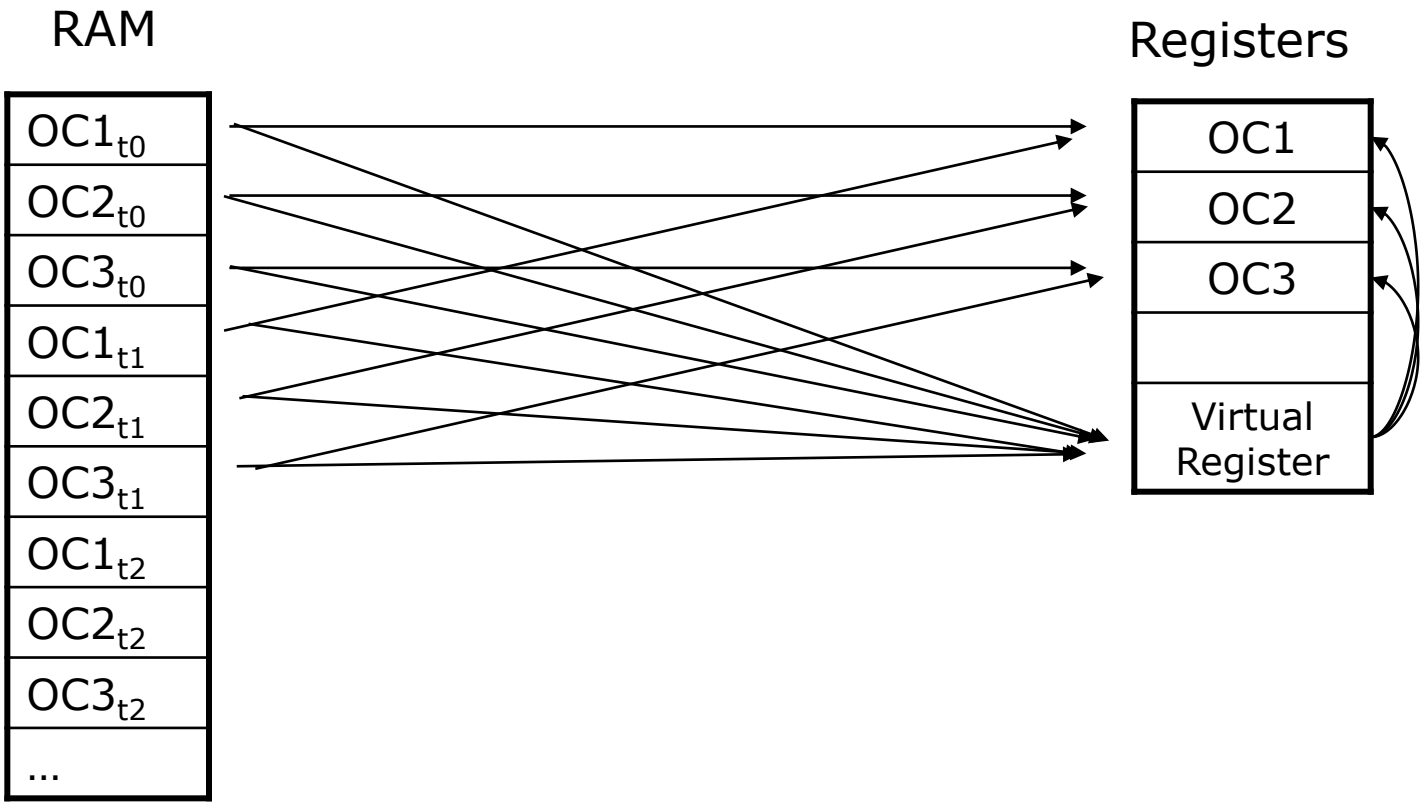
Other interrupts and DMA

- Other interrupt sources available on PWM timer
  - Each Compare match (up or down counting selectable) or capture
  - Trigger events
  - Emergency Stop
- Some events are also mapped on the DMA controller



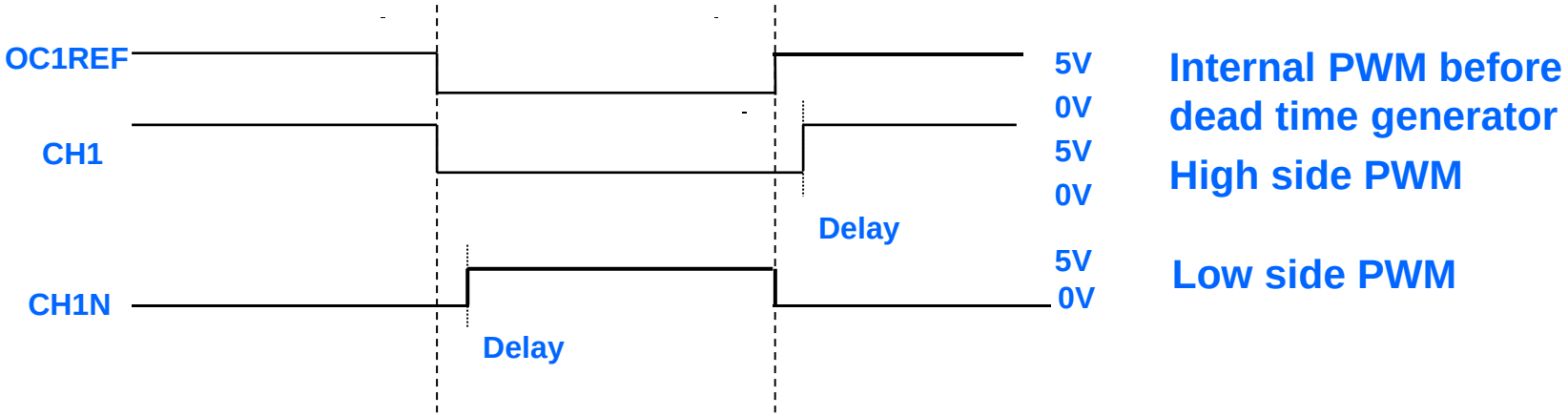
PWM's DMA burst transfer

- Allows to update several registers with a single DMA event
  - Efficient use of DMA (a single stream is required)



PWM outputs management

- Programmable hardware deadtime generation
  - 8-bit register with 13.8ns max resolution at 72MHz (from 0 to 14µs, non-linear)



- Individually selectable polarity selection
- Dedicated emergency stop input
  - Shuts down the 6 PWM outputs and issues an interrupt
  - **Asynchronous** operation (operates without clock source)

Versatile PWM redirection circuitry

Table 40. Output Control of Complementary OCx and OCxN Channels

Control Bits					Output State	
MOE bit	OSSI bit	OSSR bit	OCxE bit	OCxNE bit	OCx output state	OCxN output state
1	x	0	0	0	Output disabled	Output disabled
	x	0	0	1	Output disabled	OCREF + Polarity (OCREF xor OCxP)
	x	0	1	0	OCREF + Polarity (OCREF xor OCxP)	Output disabled
	x	0	1	1	OCREF + Polarity + dead-time	Complementary to OCREF (not OCREF) + Polarity + dead-time
	x	1	0	0	Off-State (output enabled with inactive state)	Off-State (output enabled with inactive state)
	x	1	0	1	Off-State (output enabled with inactive state)	OCREF + Polarity (OCREF xor OCxNP)
	x	1	1	0	OCREF + Polarity (OCREF xor OCxP)	Off-State (output enabled with inactive state)
	x	1	1	1	OCREF + Polarity + dead-time	Complementary to OCREF (not OCREF) + Polarity + dead-time
0	0	x	0	0	Output disabled	
	0	x	0	1		
	0	x	1	0		
	0	x	1	1		
	1	x	0	0	Off-State (output enabled with inactive state)	
	1	x	0	1		
	1	x	1	0		
	1	x	1	1		

PWM timer used as a GP timer

Motor Control (sinewave)

Motor Control (6-steps)

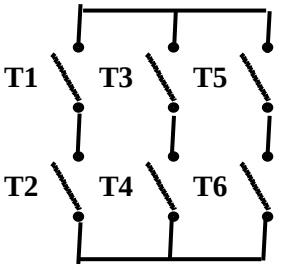
Motor Control (sinewave)

Outputs disconnected from I/O ports

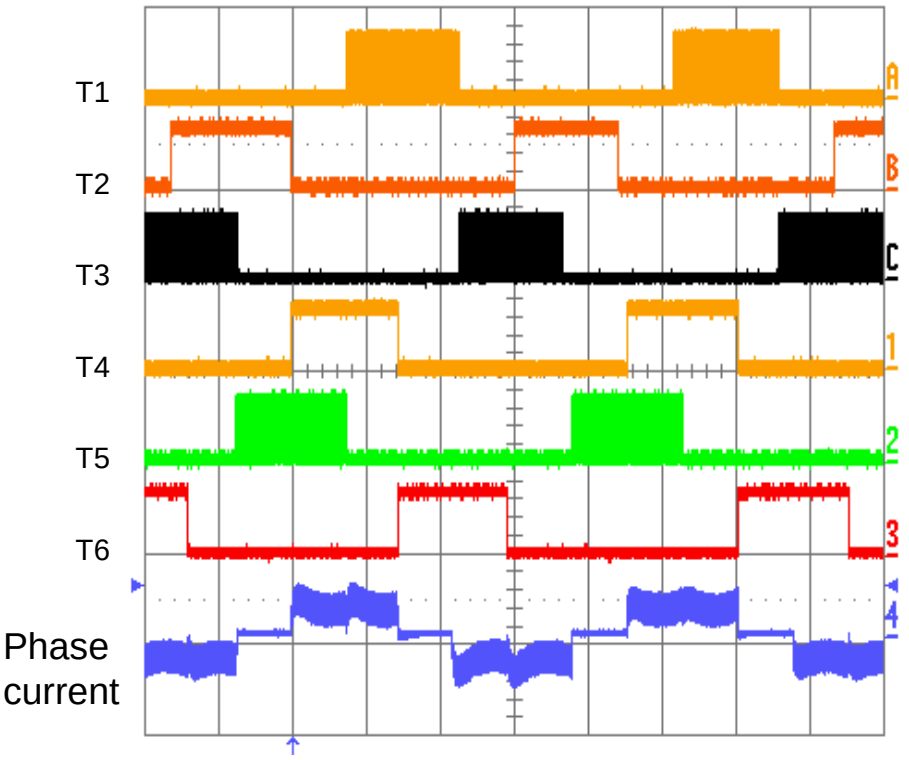
All PWMs OFF (low Z for safe stop)

Versatile PWM redirection circuitry

- Example: 6-steps (or block commutated) drives



Step	High	Low	OC1	OC1N	OC2	OC2N	OC3	OC3N
1	T1	T4	oc1ref	0	0	1	0	0
2	T1	T6	oc1ref	0	0	0	0	1
3	T3	T6	0	0	oc2ref	0	0	1
4	T3	T2	0	1	oc2ref	0	0	0
5	T5	T2	0	1	0	0	oc3ref	0
6	T5	T4	0	0	0	0	oc3ref	0



Break input

- A break event can be generated by:
  - The BRK input which has a programmable polarity and an enable bit BKE
  - The Clock Security System
- When a break occurs:
  - The MOE bit (Main Output Enable) is cleared
  - The break status flag is set and an interrupt request can be generated
  - Each output channel is driven with the level programmed in the OISx bit
- Break applications:
  - If the AOE is Reset, the MOE remains low until you write it to ‘1’ again
    - Normally used for security with break input connected to an alarm feedback from power stage, thermal sensors or any security components.
  - If the AOE (Automatic Output Enable) bit is set, the MOE bit is automatically set again at the next update event UEV
    - Typically be used for cycle-by-cycle current regulation

Smoke inhibit protections

- Safety critical registers can be “locked”, to prevent power stage damages (software run-away,…)
  - Dead time, PWM outputs polarity, emergency input enable,…
- All target registers are read/write until lock activation (and then read-only if protected)
  - Once the two lock bits are written, they cannot be modified until next MCU reset (write-once bits)
- Three programmable write protection levels
  - Level1: Dead Time and Emergency enable are locked.
  - Level2: Level1 + Polarities and Off-state selection for run and Idle state are locked.
  - Level3: Level2 + Output Compare Control and Preload are locked.
- GPIO configuration can be locked to avoid having the PWM alternate function outputs reprogrammed as standard outputs

Debug feature

- Motor control applications are usually tricky to debug using breakpoints
  - Standard breakpoints may damage the power stage
  - Closed loop systems can hardly be stopped and re-started

- A configuration bit allows to program the behavior of the PWM timer upon breakpoint match
  - Normal mode: the timer continues to operate normally
    - May be dangerous in some case since a constant duty cycle is applied to the inverter (interrupts not serviced)
  - Safe mode: the timer is frozen and PWM outputs are shut down
    - Safe state for the inverter. The timer can still be re-started from where it stops.

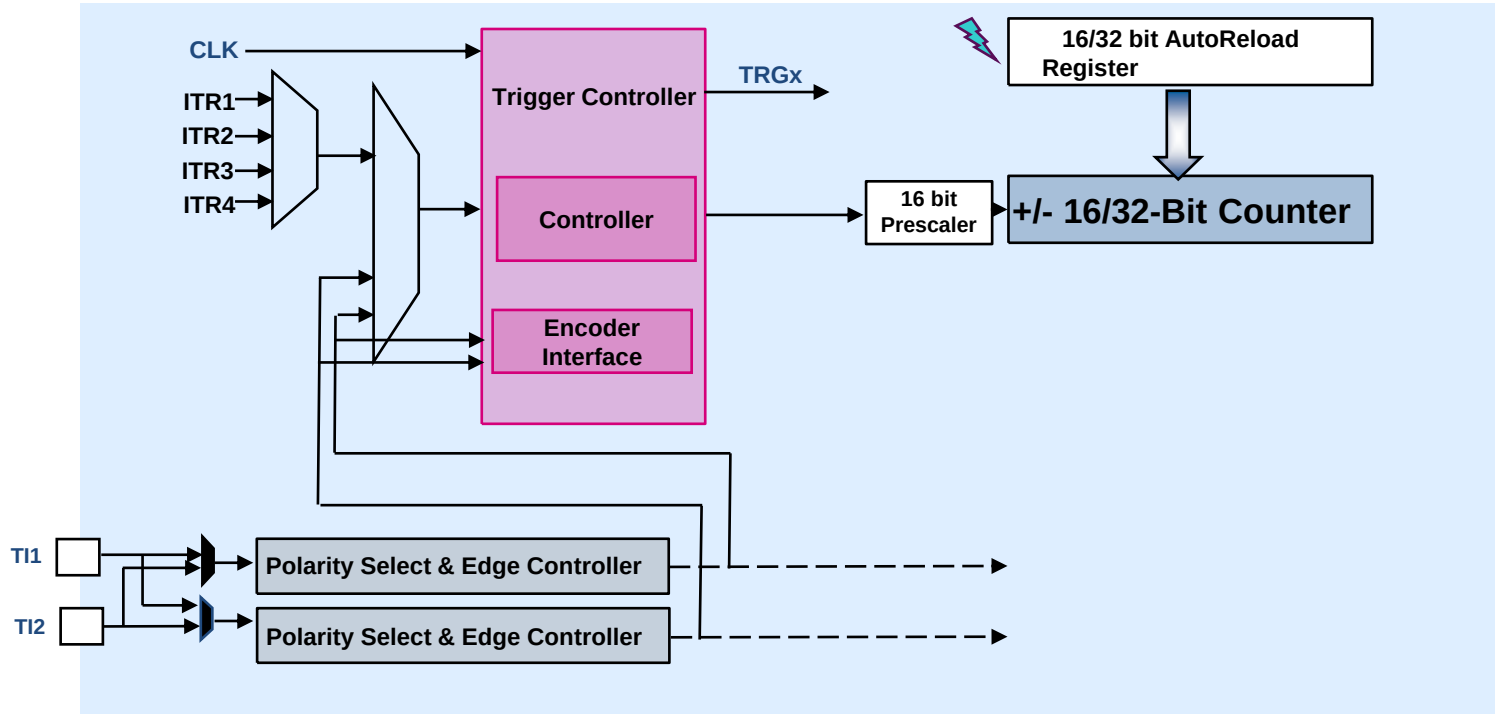
Peripherals for advanced motor control

- PWM generation
- **Speed / position feedback**
- Multi timer configuration
- Analog to Digital converter
- Other inbuilt peripherals (DMA, connectivity)

Speed Feedback

- Handled by the general purpose timers in dedicated modes
  - These functions are available on most timers
- Hall sensors
  - Hall Sensor interface (XOR’ed inputs)
- Encoder
  - Encoder modes 1, 2 & 3 (2x, 4x)
- Tacho feedback
  - Clear on capture to measure exact period

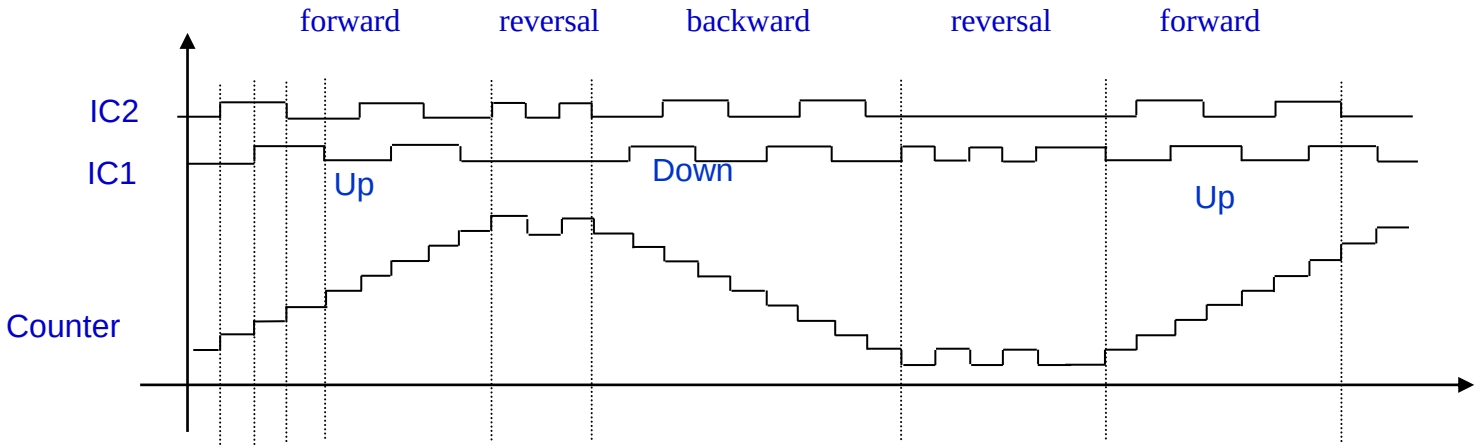
TIM Block Diagram in encoder mode



Interfacing a TIM timer with an encoder

- Encoders and STM32 connection example:
  - An incremental encoder can be connected directly to the MCU without external interface logic.
  - The third encoder output which indicates the mechanical zero position (Z or index), may be connected to an external interrupt and trigger a counter reset

Example of counter operation in Encoder Interface mode



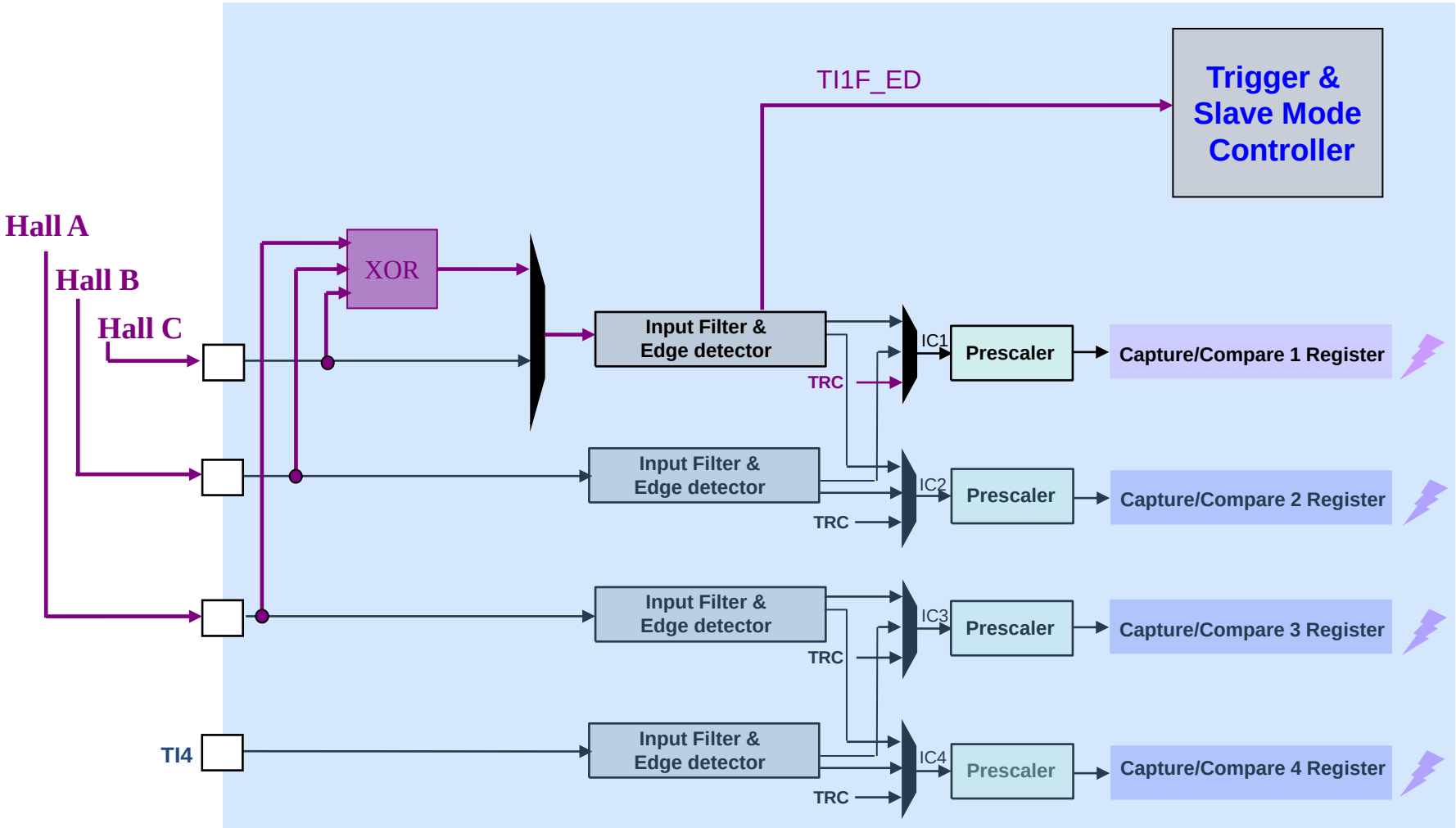
Key encoder features

- Programmable counting rate
- x4: normal mode, all edges active
- a 1000 lines encoder will give 4000 counts per revolution
- x2: counts on input A (or B) only, but direction still determined with A and B
- “velocity mode”: encoder clock can be further prescaled if needed

- Programmable encoder resolution
- When programming the autoreload register with the number of counts per revolution, the counter register directly holds the angle or the position
- No need to do the difference vs previous counter value
- If set to 0xFFFF, can be made compatible with previous designs using a free-running counter

- Possibility to generate one/multiple interrupts per revolution:
- once every 360°
- once 60°, 90°,… (depending on autoreload register setting)

Hall sensor Interface



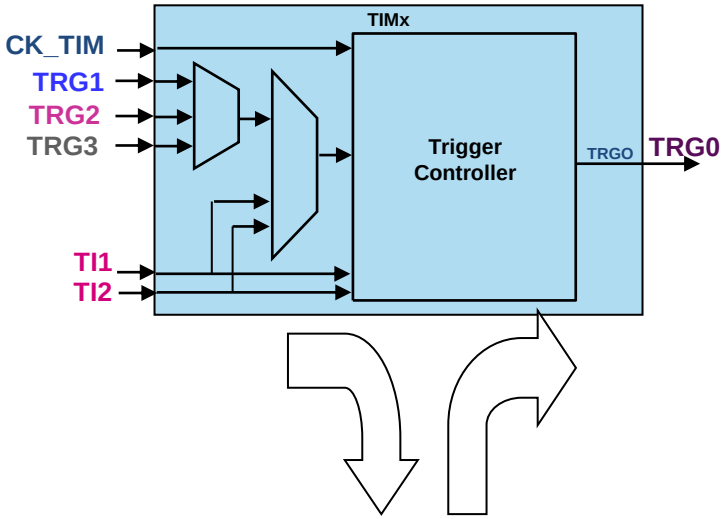
Peripherals for advanced motor control

- PWM generation
- Speed / position feedback
- **Multi timer configuration**
- Analog to Digital converter
- Other inbuilt peripherals (DMA, connectivity)

Timer Link system

- The three general purpose and the advanced timers are linked together and can be synchronized or chained, thanks to a Trigger output and several selectable trigger inputs.
- For TIM2:0, the input pins(TI1 and TI2) can also be used as triggers

Trigger inputs



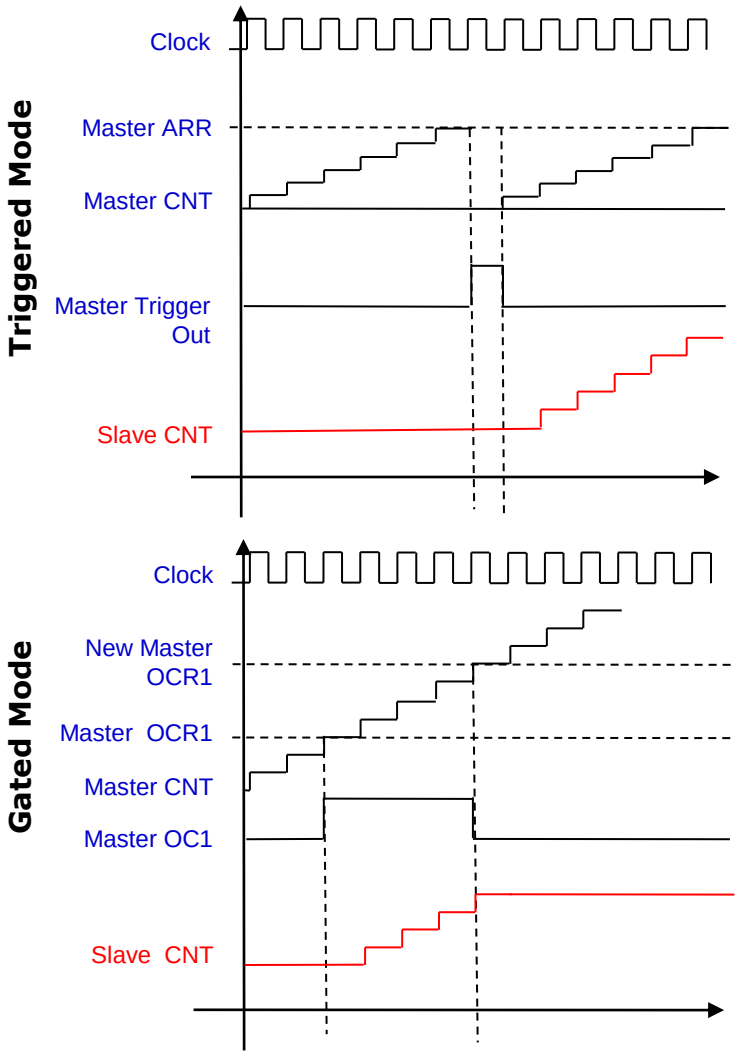
Trigger outputs

Timer control signals: clock, reset, update, enable,…

Synchronization Mode Configuration

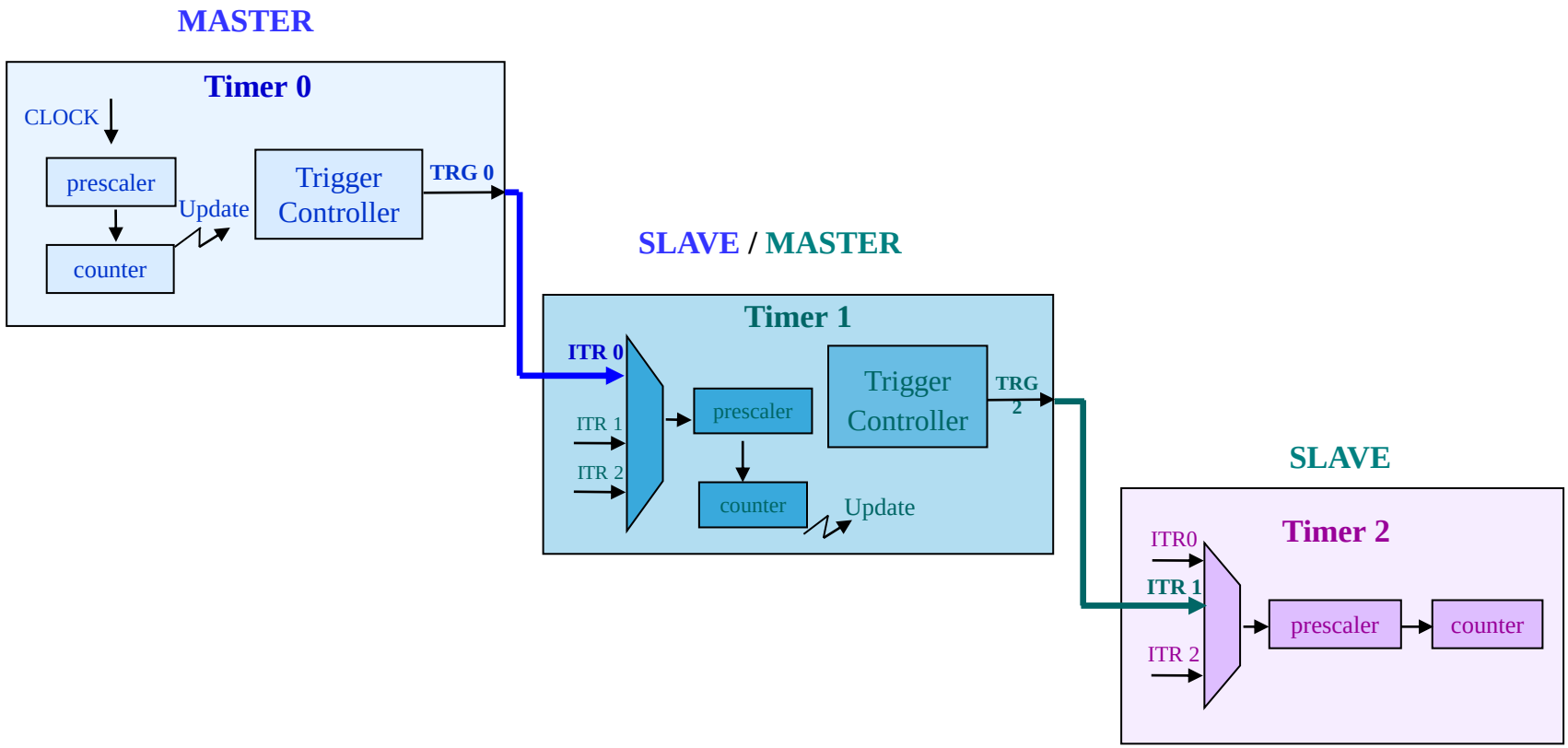
- When in **master** mode, the timer can output one of these:
  - Counter reset
  - Counter enable
  - Update event
  - Output Compare signal

- When configured as **slave**, the timer can work in the following modes:
  - Triggered
  - Gated
  - Reset
  - External clock

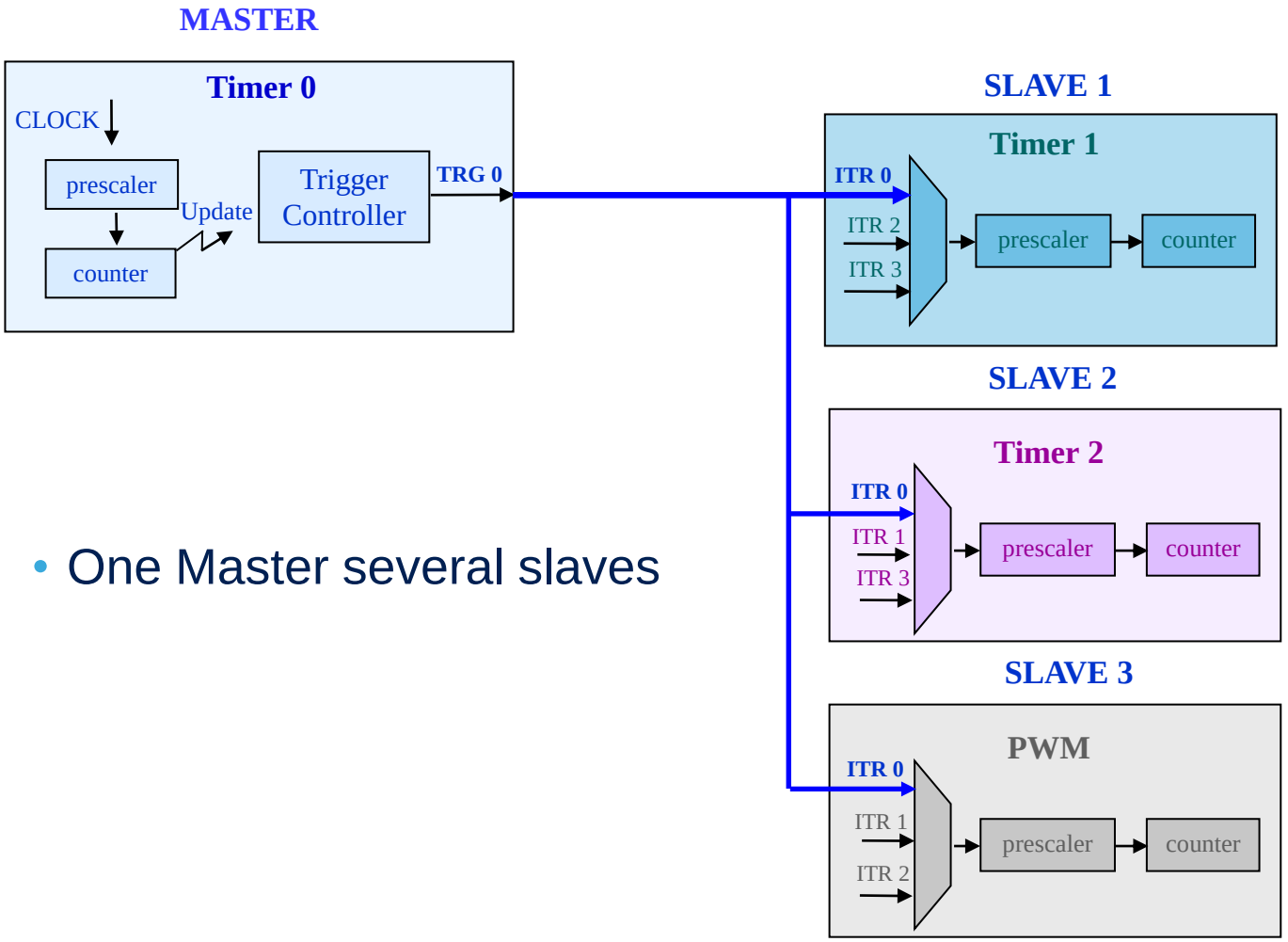


Example 1/3: chained timers

- Cascade mode (for instance, chained time bases)



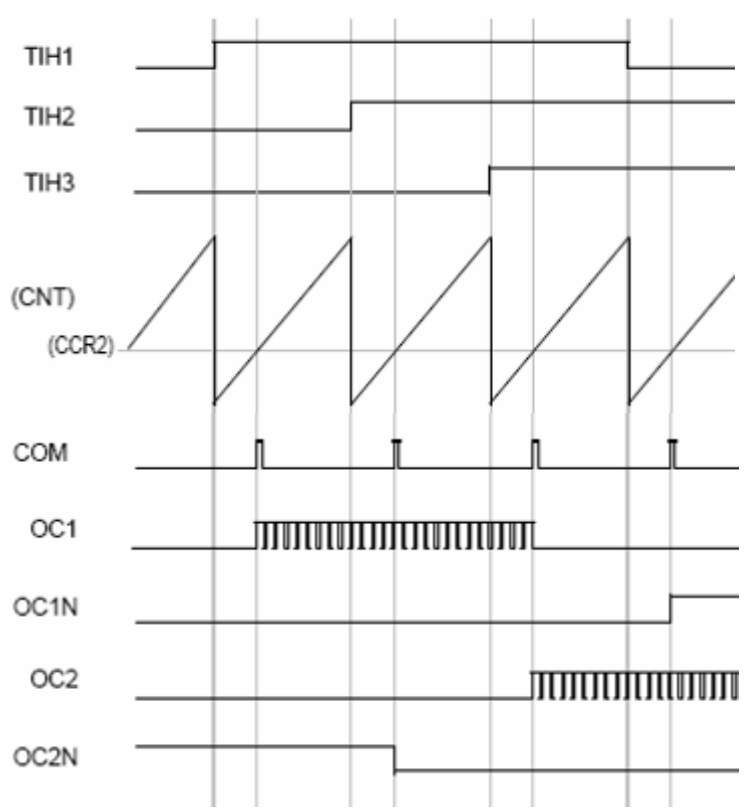
Examples 2/3: synchronized start

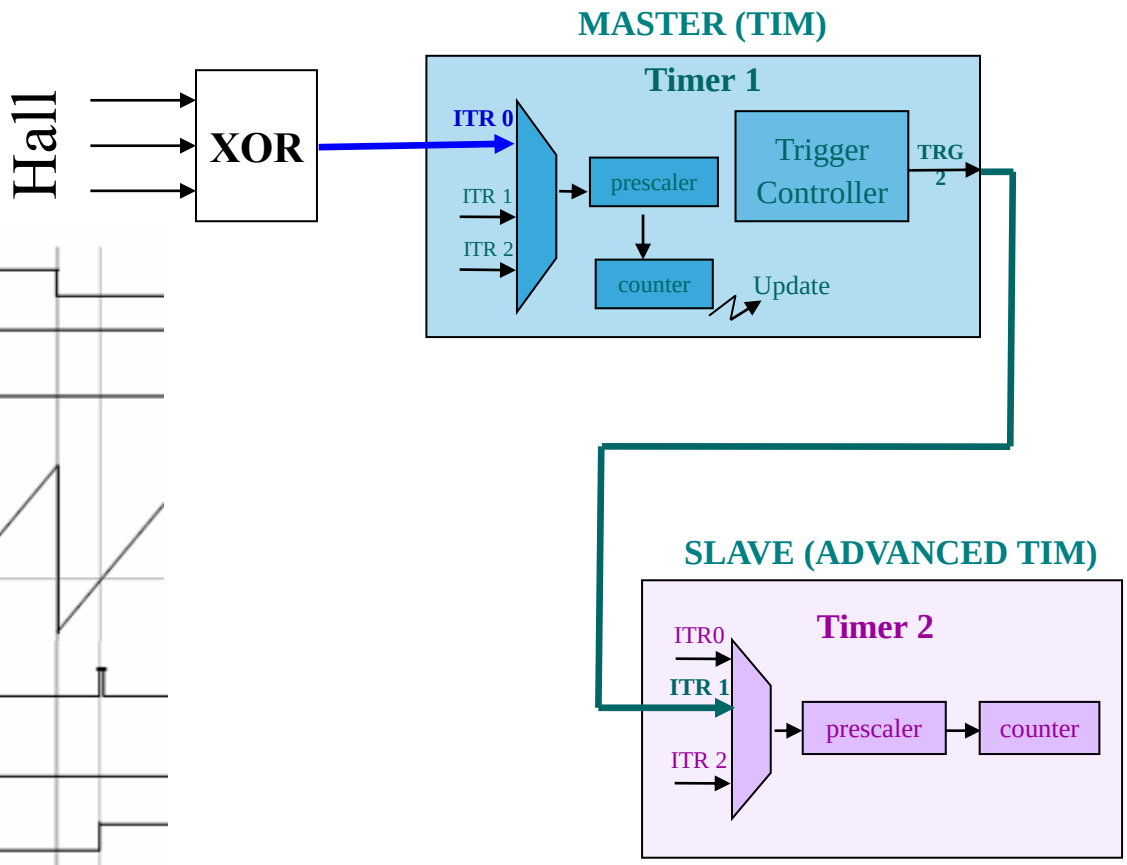


- One Master several slaves

Examples 3/3: block commutation

- A TIM timer handles Hall feedback and triggers an advanced timer for step commutation





Peripherals for advanced motor control

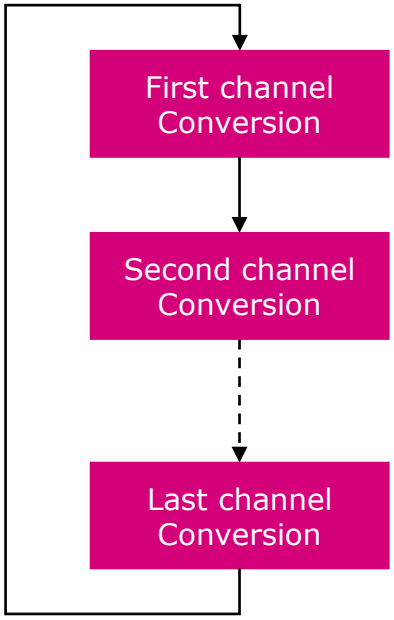
- PWM generation
- Speed / position feedback
- Multi timer configuration
- **Analog to Digital converter**
- Other inbuilt peripherals (DMA, connectivity)

ADC Features (1/3)

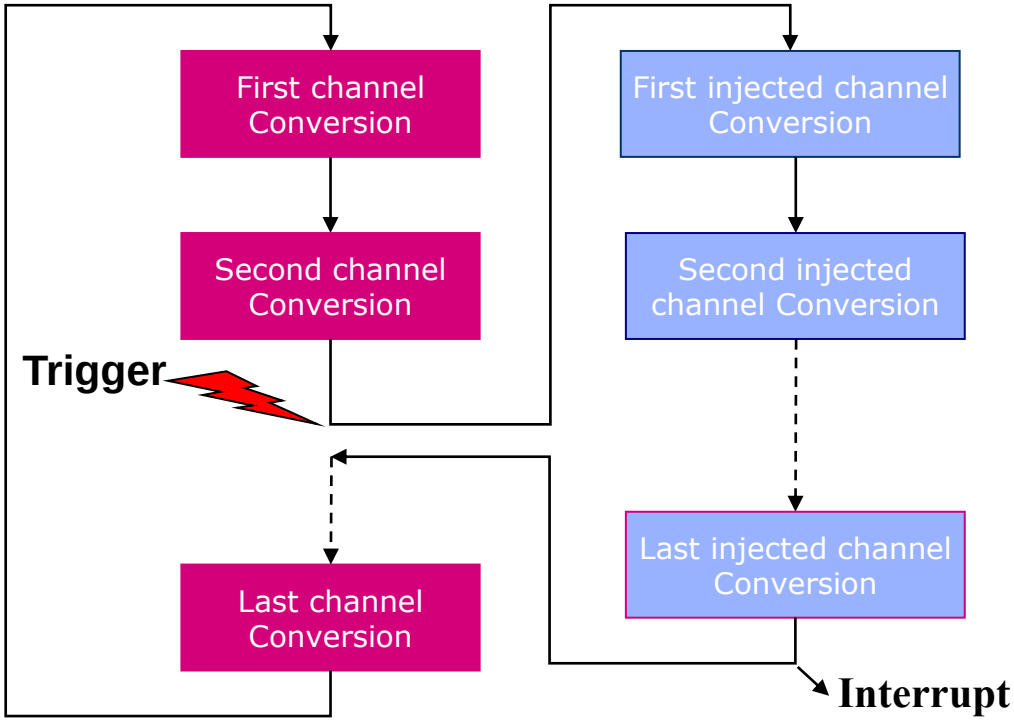
- ADC conversion rate 1 MHz and 12-bit resolution
- *1µs conversion time at 56 MHz*
- *1.17µs conversion time at 72 MHz*
- Conversion range: 0 to 3.6 V
- ADC supply requirement: 2.4V to 3.6 V
- ADC input range: VREF- ≤ VIN ≤ VREF+ (VREF+ and VREF- available only in LQFP100 package)
- Dual mode (on devices with 2 ADCs): 8 conversion mode
- Up to 18 multiplexed channels:
- 16 external channels
- 2 internal channels: connected to Temperature sensor and internal reference voltage (VREFINT=1.2V)
- Channels conversion groups:
- Up to 16 channels regular group
- Up to 4 channels injected group
- Single and continuous conversion modes

ADC Injected Conversion

- Regular Scan mode

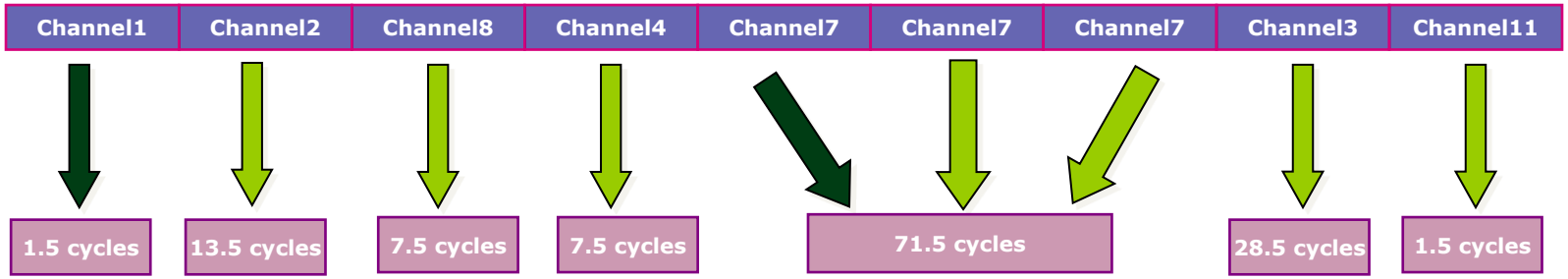


- Scan mode with Injected high priority trigger



ADC Features (2/3)

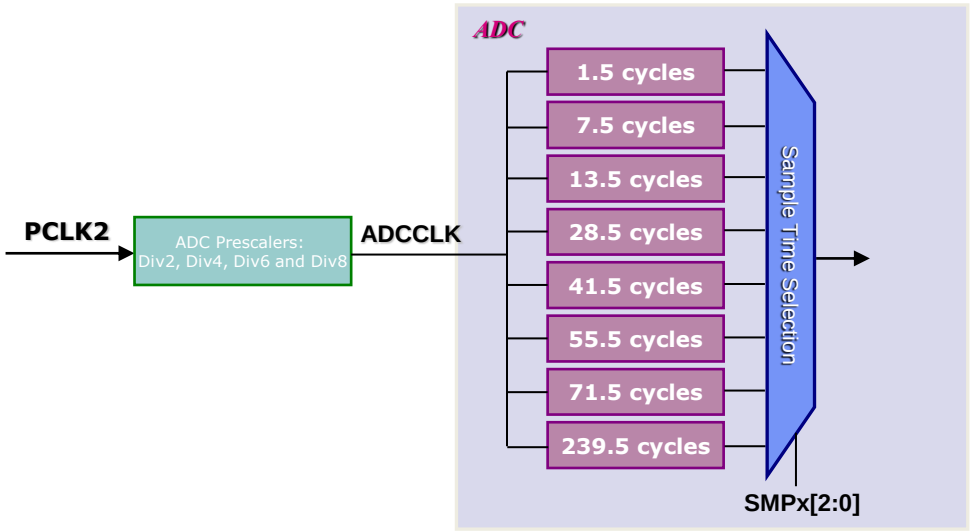
- Analog Watchdog(s) (1 channel or all regular or all injected)
- Sequencer-based scan mode
- Any channel, any order (e.g. Ch3, Ch2, Ch11, Ch11, Ch3)
- up to 16 regular conversion (transferred by DMA)
- up to 4 injected conversion stored in internal registers



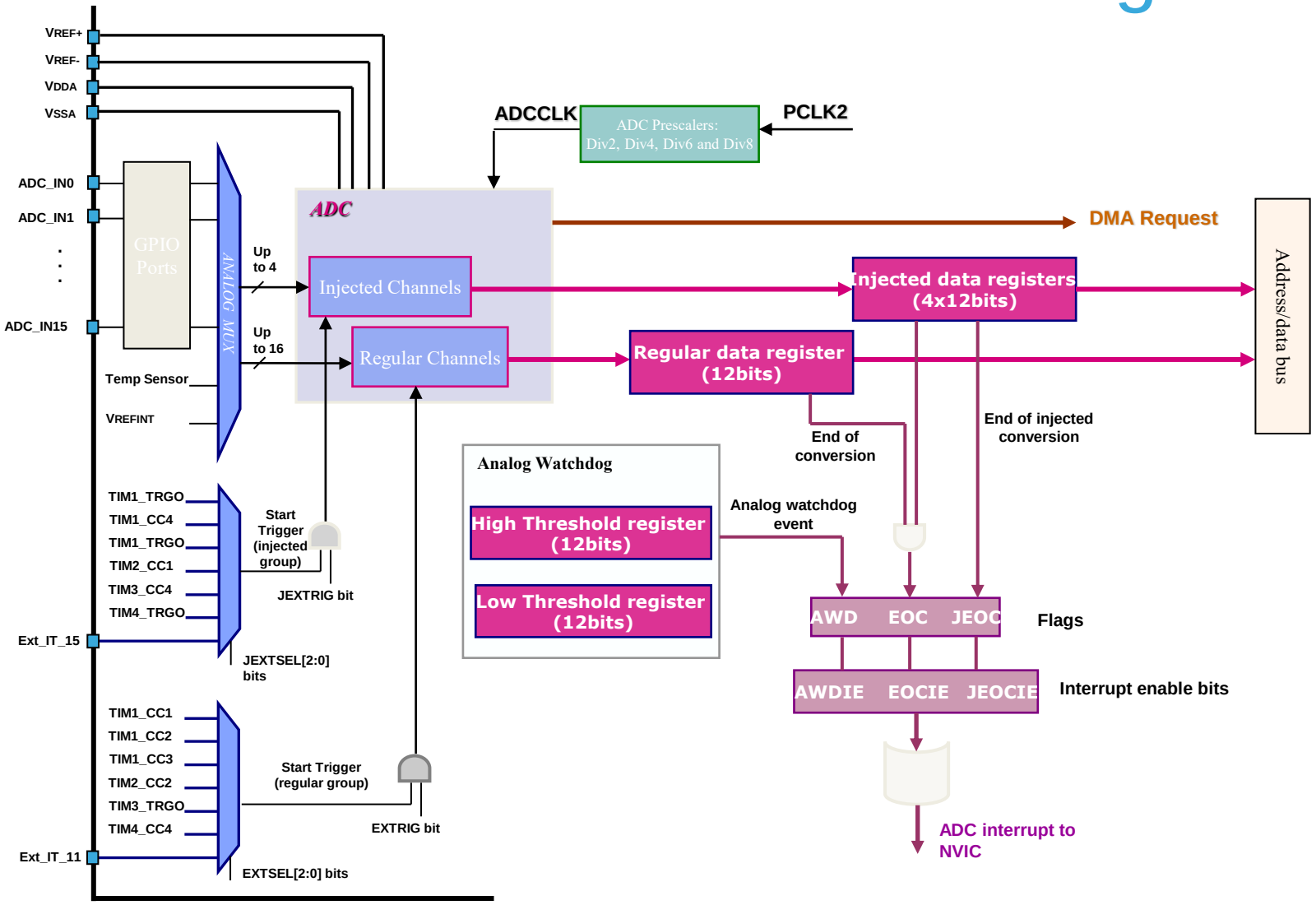
- Multiple trigger sources for both regular and injected conversion
- Each group can be started by 6 events from the 4 timers (compare, over/underflow)
- External event and software trig also available

ADC Features (3/3)

- Left or right Data alignment with built-in data coherency
- 4 offset compensation registers
- Compensates external conditioning components offsets (such as Operational Amplifiers). Provides signed results if needed.
- Channel-by-channel programmable sampling time to be able to convert signals with various impedances
- From 1µs (for Rin < 1.2 kOhm) to 18µs (Rin < 350 kOhm), 8 values

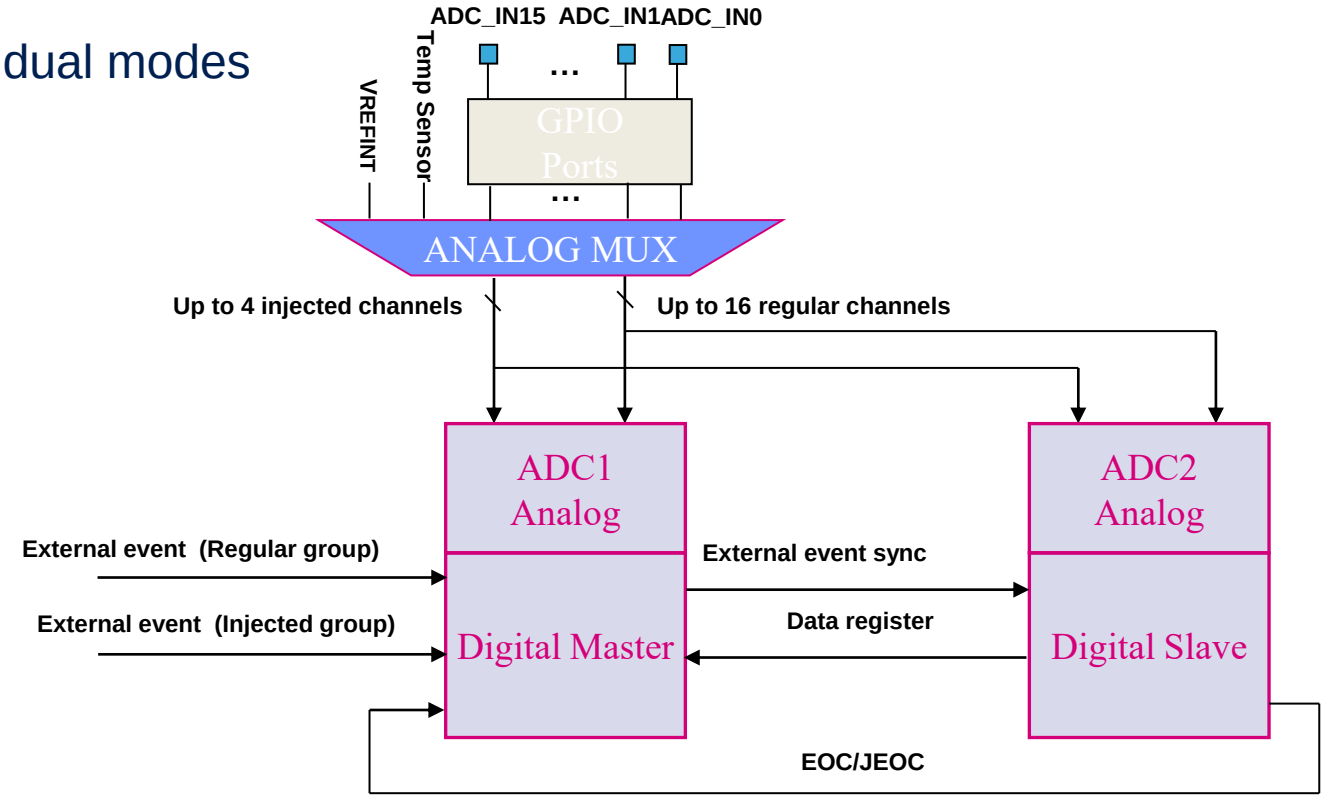


ADC Block Diagram



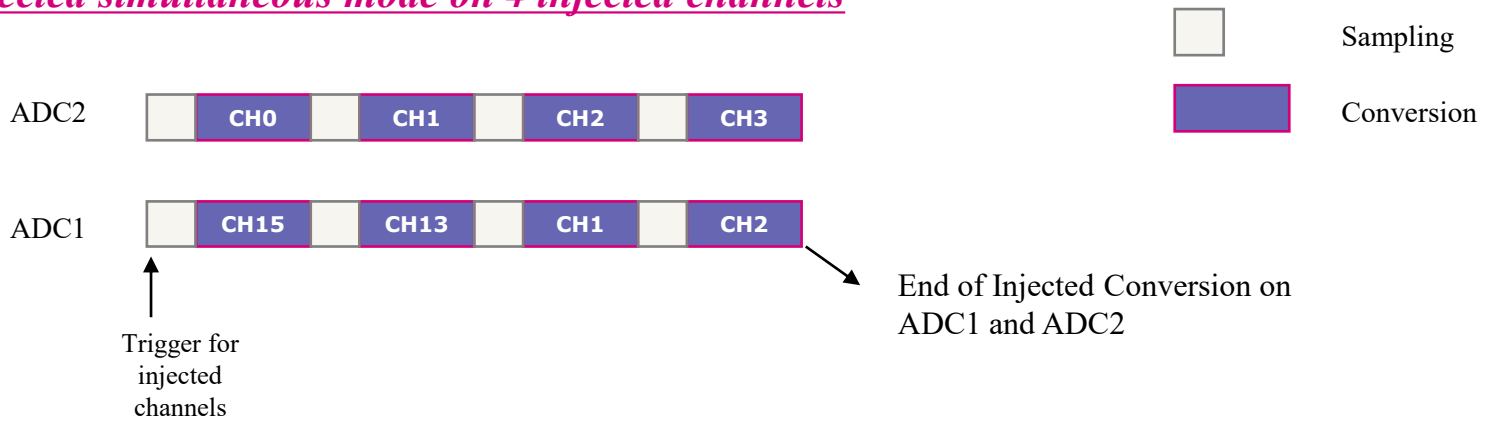
ADC dual modes (1/2)

- Available in devices with two ADCs (Performance line)
  - ADC1 and ADC 2 can work independently or coupled (master/slave)
- 8 ADC dual modes

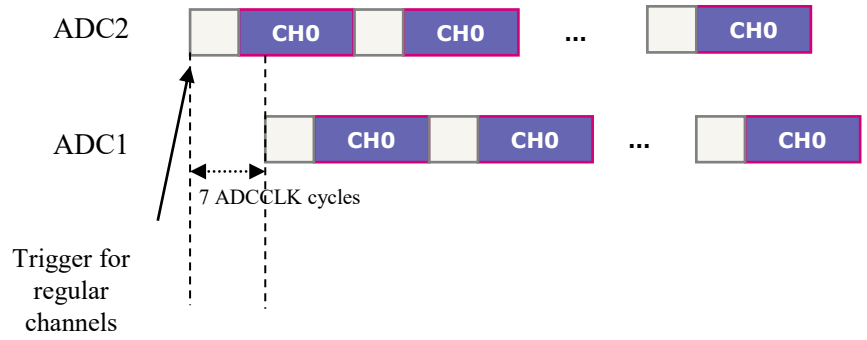


ADC dual modes example (2/2)

Injected simultaneous mode on 4 injected channels



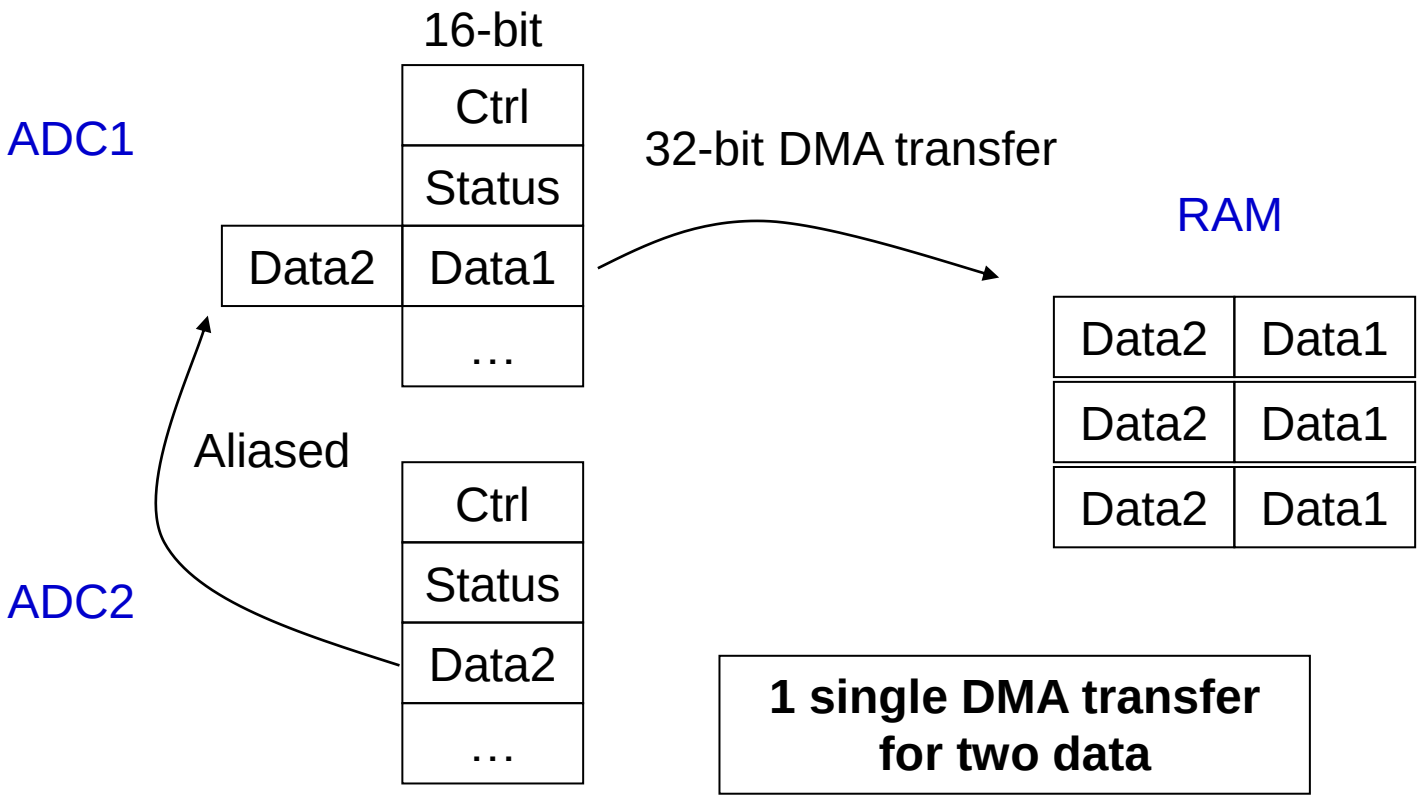
Fast Interleaved mode on 1 regular channel in continuous conversion mode



Up to 2 MSps data throughput (DMA-based)

DMA transfers in interleaved mode

- Interleaved mode: continuous conversions of the two ADCs on the same channel with aliased data register

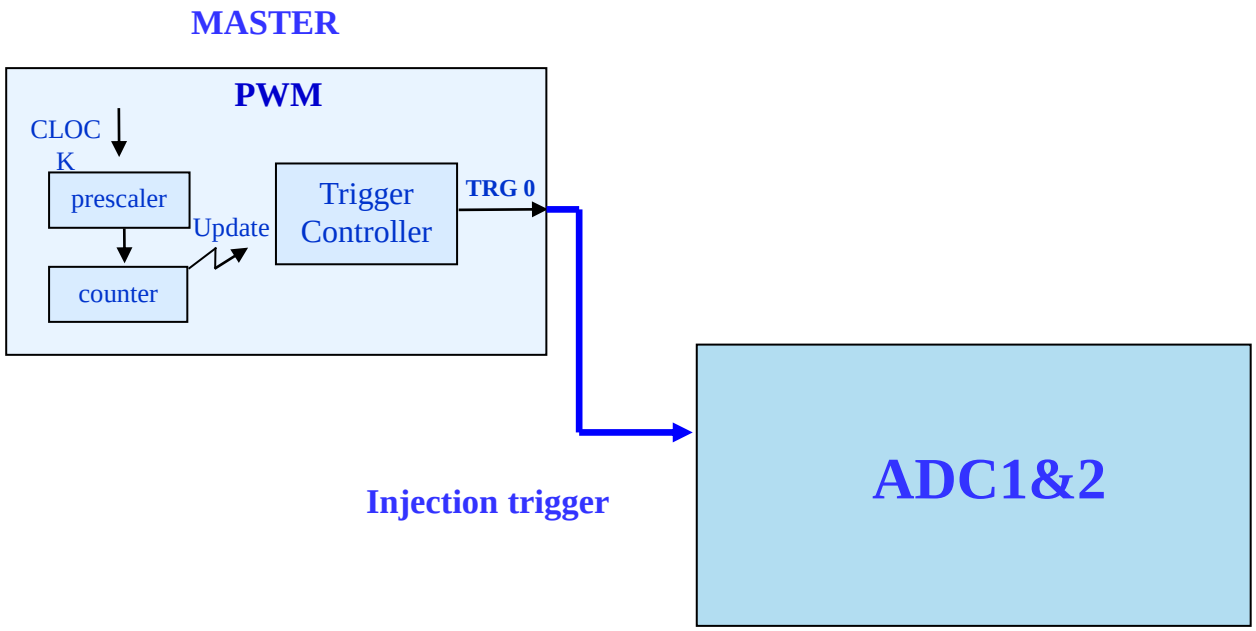


ADC synchronization in STM32

- Done thanks to a synchronization unit embedded in the PWM timer.
- 2 options available:
  - Direct synchronization on PWM crest, valley, or both.
  - Delayed synchronization with the 4th Compare channel
- The ADC results can be then processed with an end of conversion interrupt or transferred by DMA.

Direct synchronization

- The PWM timer “update” signal triggers Simultaneous injected conversions on both ADCs
  - No error due to sequential phase sampling



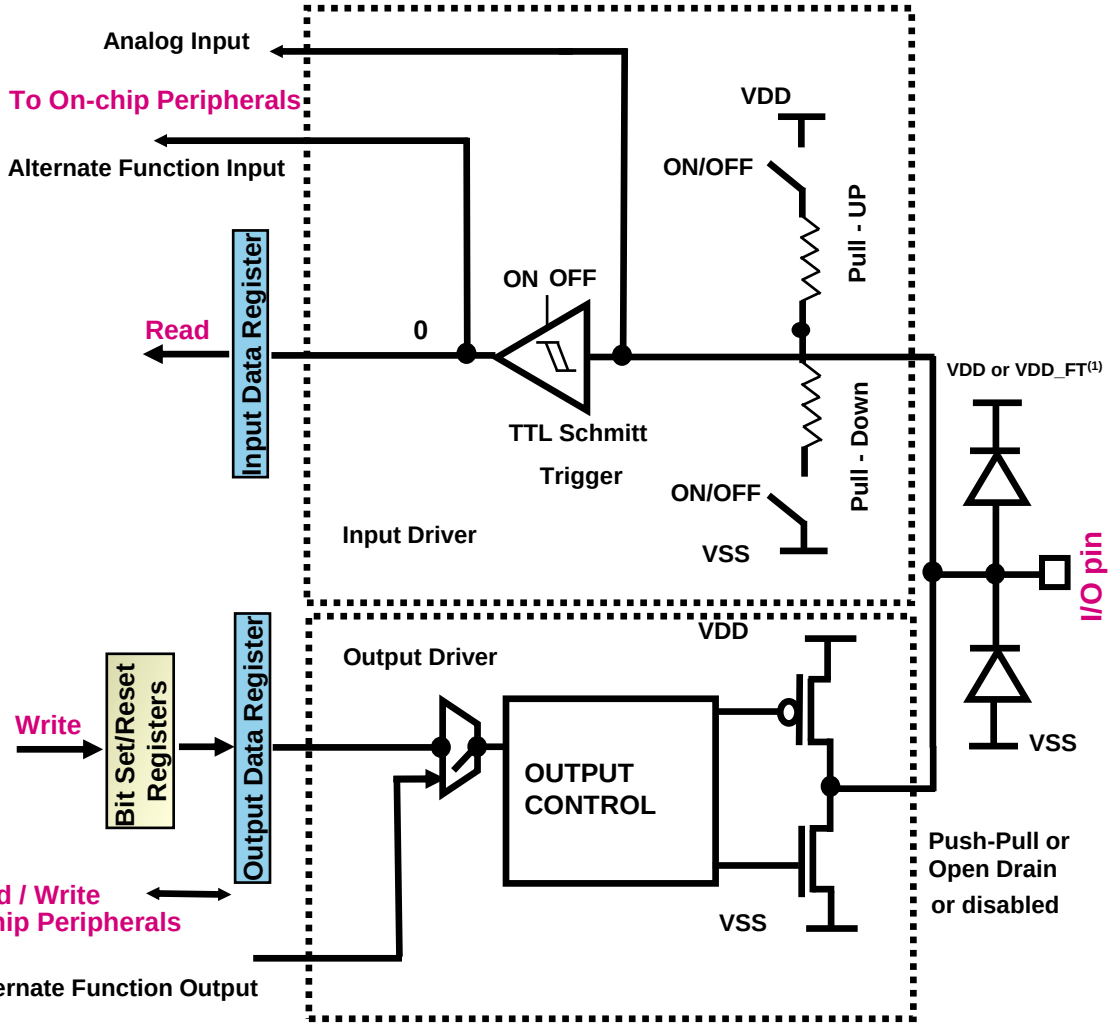
GPIO Features

GPIO Features

- Up to 80 multifunction bi-directional I/O ports available: 80% IO ratio
- Standard I/Os 5V tolerant
- The GPIOs can sink or source 25mA (total currents sunk is 150mA)
- 36-42 MHz Toggling (84 MHz / 90 MHz / 100 MHz)
- Configurable Output Speed up to 50 MHz (84 MHz / 90 MHz / 100 MHz)
- Up to 24 Analog Inputs
- Alternate Functions pins (like USARTx, TIMx, I2Cx, SPIx, CAN, USB…)
- All GPIOs can be set-up as external interrupt (up to 16 lines at time)
- 1-4 I/Os can be used as Wake-Up from STANDBY (PA0)
- One I/O can be set-up as Tamper Pin (PC13)
- All Standard I/Os are shared in ports (GPIOA..GPIOF)
- Atomic Bit Set and Bit Reset using BSRR and BRR registers
- Locking mechanism to avoid spurious write in the IO registers
- When the LOCK sequence has been applied on a port bit, it is no longer possible to modify the configuration of the port bit until the next reset (no write access to the CRL and CRH registers corresponding bit).

GPIO Configuration Modes

Configuration Mode	CNF1	CNF0	MOD1	MOD0
Analog Input	0	0	00	
Input Floating **(Reset State)**	0	1		
Input Pull-Up	1	0		
Input Pull-Down	1	0		
Output Push-Pull	0	0	01: 10 MHz 10: 2 MHz 11: 50 MHz	
Output Open-Drain	0	1		
AF Push-Pull	1	0		
AF Open-Drain	1	1		



(1) ***VDD for standard I/Os and VDD_FT is a potential specific to five-volt tolerant I/Os and different from VDD.***

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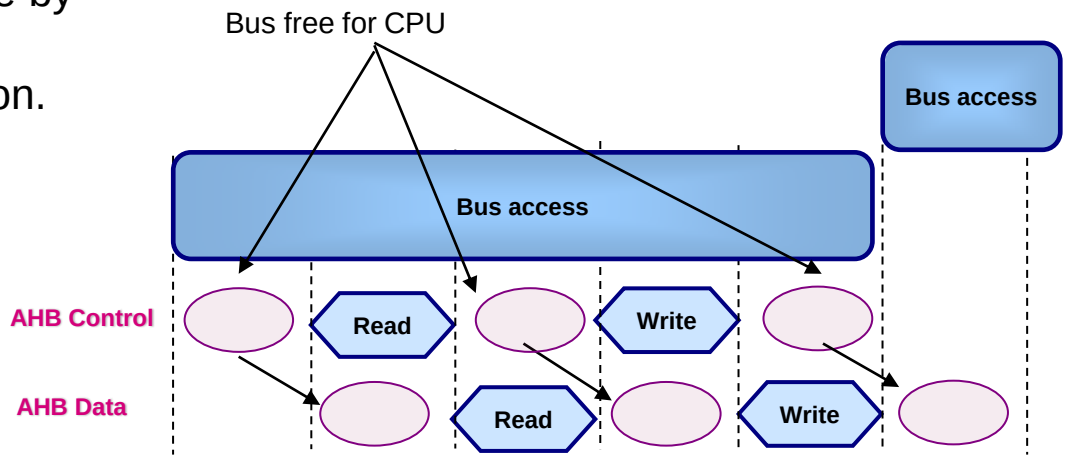
- **Other inbuilt peripherals (DMA, connectivity)**

DMA & features

- Standalone data-transfer controller
- 5-16 independently configurable channels: hardware requests or software trigger on each channel
- Software programmable priorities: Very high, High, Medium or Low (Hardware priority in case of equality)
- Programmable and Independent source and destination transfer data size: Byte, HalfWord or Word
- 3 event flags for each channel: DMA Half Transfer, DMA Transfer complete and DMA Transfer Error
- Memory-to-memory, peripheral-to-memory, memory-to-peripheral transfers and peripheral-to-peripheral transfer types
- Faulty channel is automatically disabled in case of bus access error
- Programmable number of data to be transferred: up to 2x 65535
- Support for circular buffer management and dual-buffer

DMA and Bus occupation

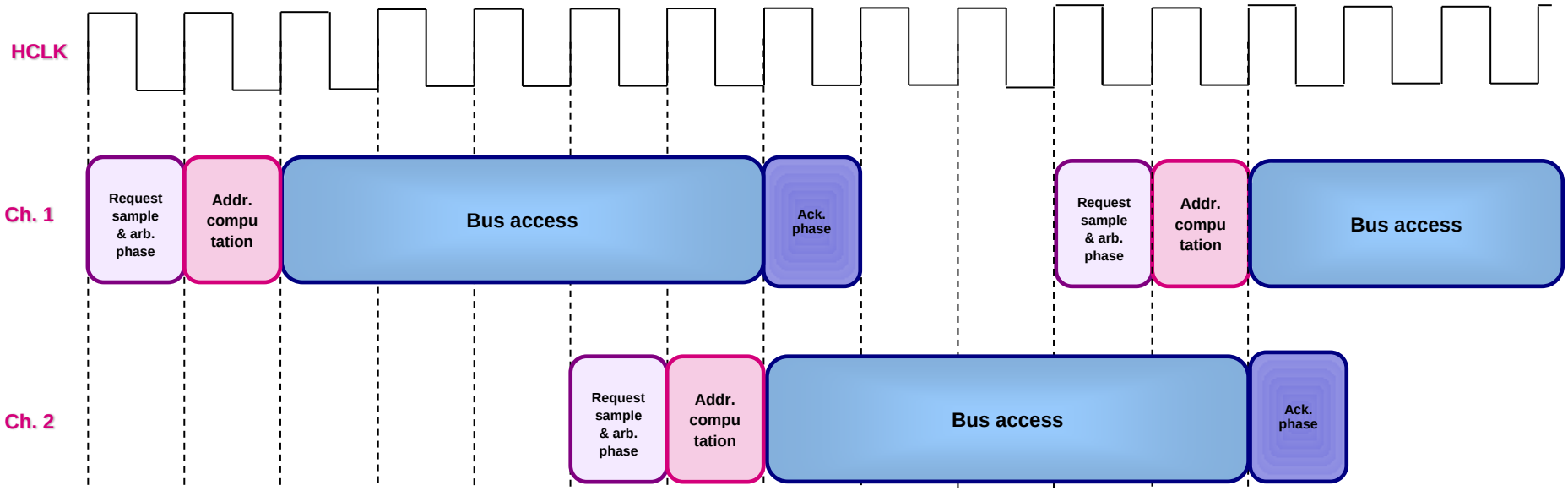
- Request, arbitration and acknowledgement operations are done outside AHB system bus, so the bus is not occupied during those phases
- One DMA access takes 2 cycles (on AHB): the system bus can not be totally freeze by DMA as at least 3 cycles are left to the CPU during one DMA transaction.



- Current DMA controller compared to others which permit burst transfer have nearly the same system bus occupation rate. However, it doesn't freeze the bus for many cycles consecutively as it is the case with the burst mode: better performance with many small data transfer without blocking the bus

DMA Latency: 2 transfers

- To improve the DMA performances, a new request can be served while the previous one is running: if a request is active and others are pending, the new request sample & arbitration phase is performed during AHB bus access of the current request. The winning request for AHB bus access will start immediately after the end of the current request's AHB Bus access.



- If source or destination is on APB, the transfer takes more cycles (1+N for APB:AHB = N:1)

Connectivity

- Different STM32 families are equipped with various communication peripherals and other interfaces:
  - USART (up to 8x)
  - SPI (up to 3x)
  - CAN (up to 2x)
  - Ethernet MAC
  - USB OTG (up to 2x)
  - I2C (up to 3x)
  - I2S (2x), SAI
  - SDIO
  - Camera
- You can find more details in datasheet or dedicated training sessions

STM32 F3
embedded analog

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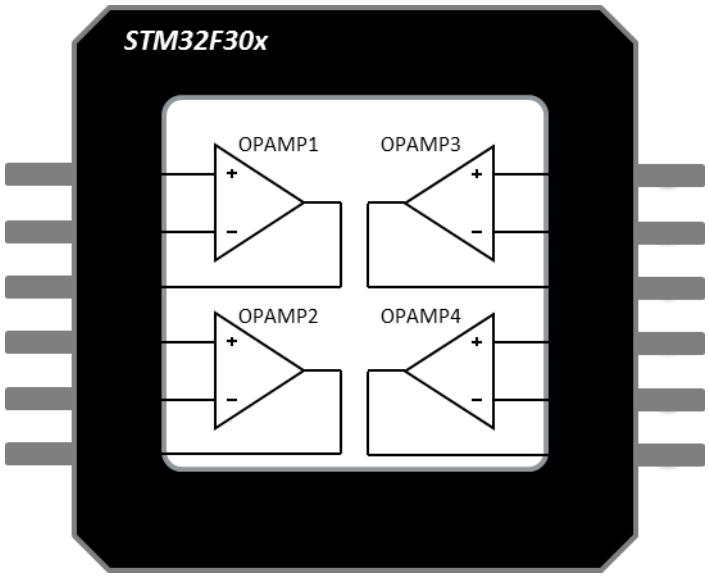
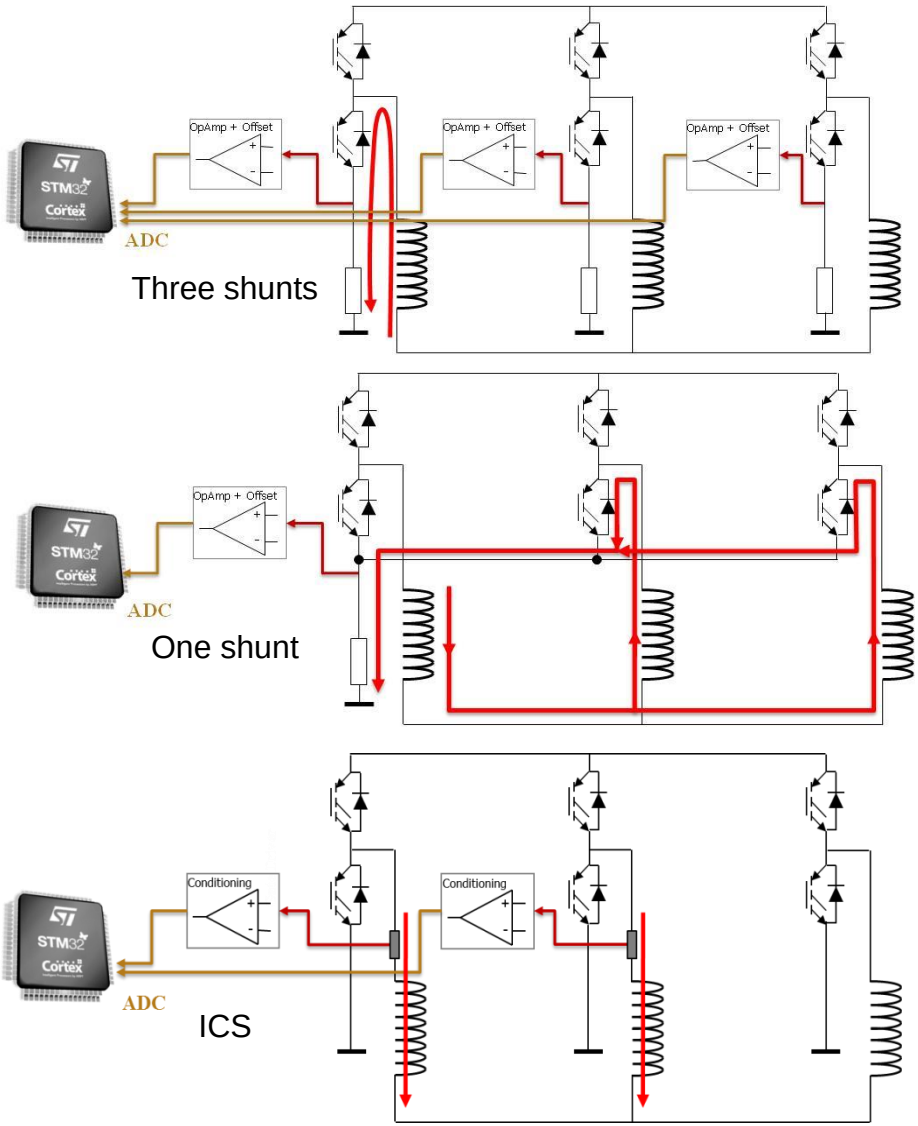
Operational amplifier

Up to four embedded PGA for current sensing conditioning



Characteristics

- 8.2 MHz bandwidth
- 4.7V/us slew rate
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be x2, x4, x8 or x16.
- Registers lock



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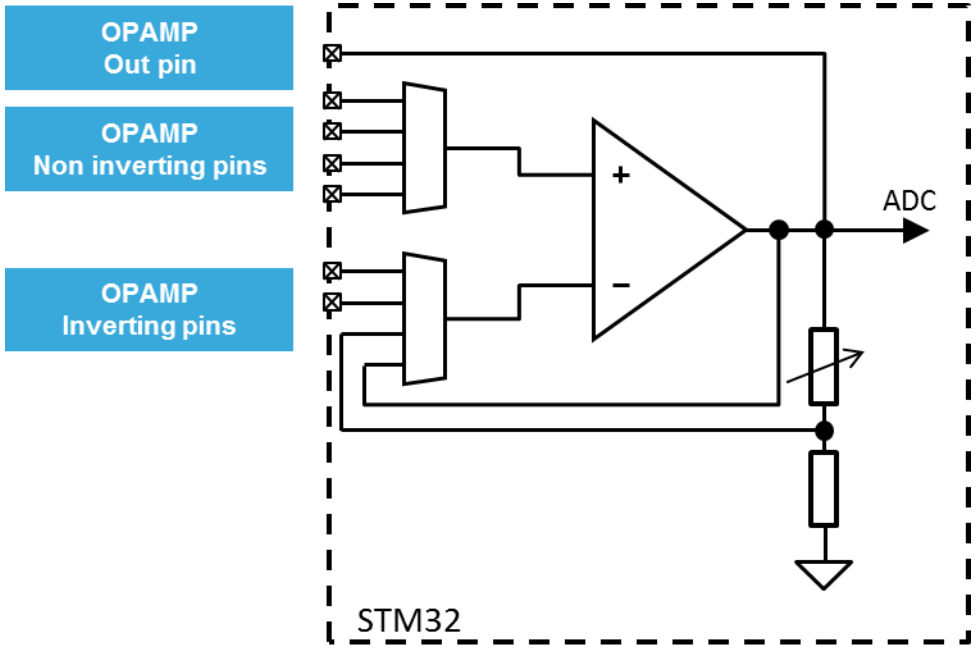
Operational amplifiers

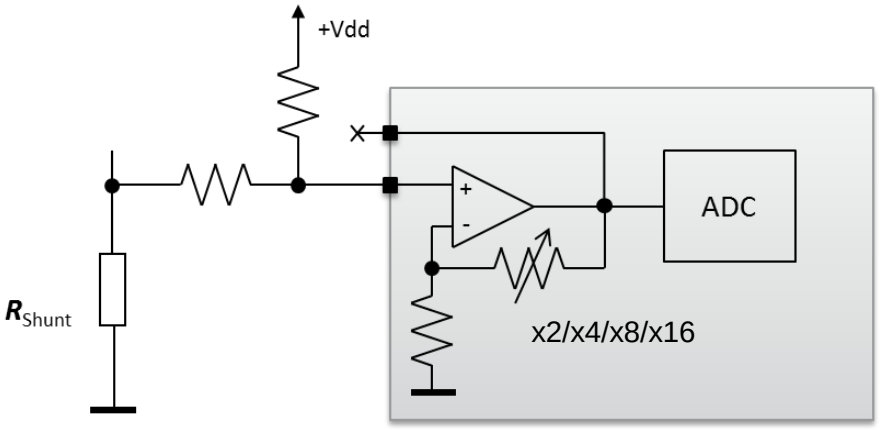
Available pins



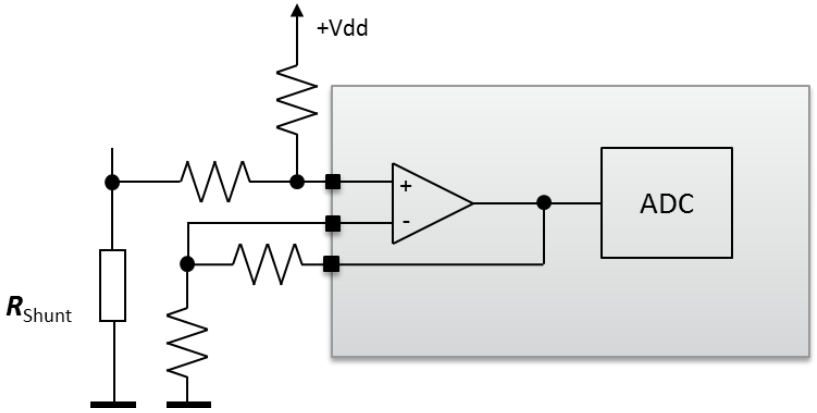
OPAMP1 Inverting pins	OPAMP1 Non inverting pins	OPAMP1 Out pin	OPAMP2 Inverting pins	OPAMP2 Non inverting pins	OPAMP2 Out pin
PA3, PC5	PA1, PA7, PA3, PA5	PA2	PA5, PC5	PA7, PB14, PB0, PD14	PA6
OPAMP3 Inverting pins	**OPAMP3 Non inverting pins**	**OPAMP3 Out pin**	**OPAMP4 Inverting pins**	**OPAMP4 Non inverting pins**	**OPAMP4 Out pin**
PB2, PB10	PB0, PB13, PA1, PA5	PB1	PB10, PD8	PB13, PD11, PB11, PA4	PB12

Operational amplifier

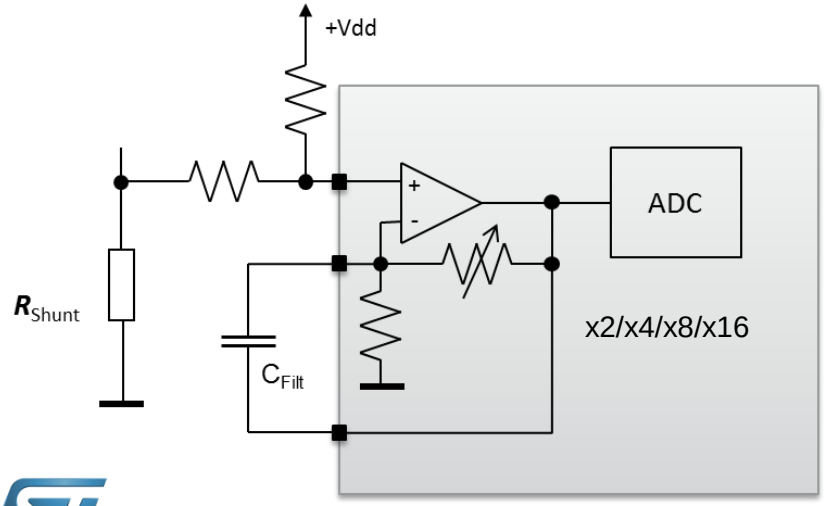
Allowed configurations



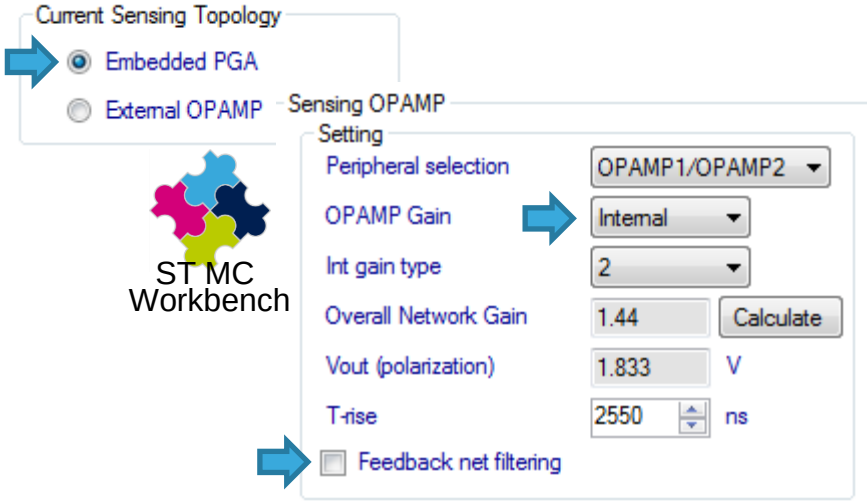
Internal gain



External gain

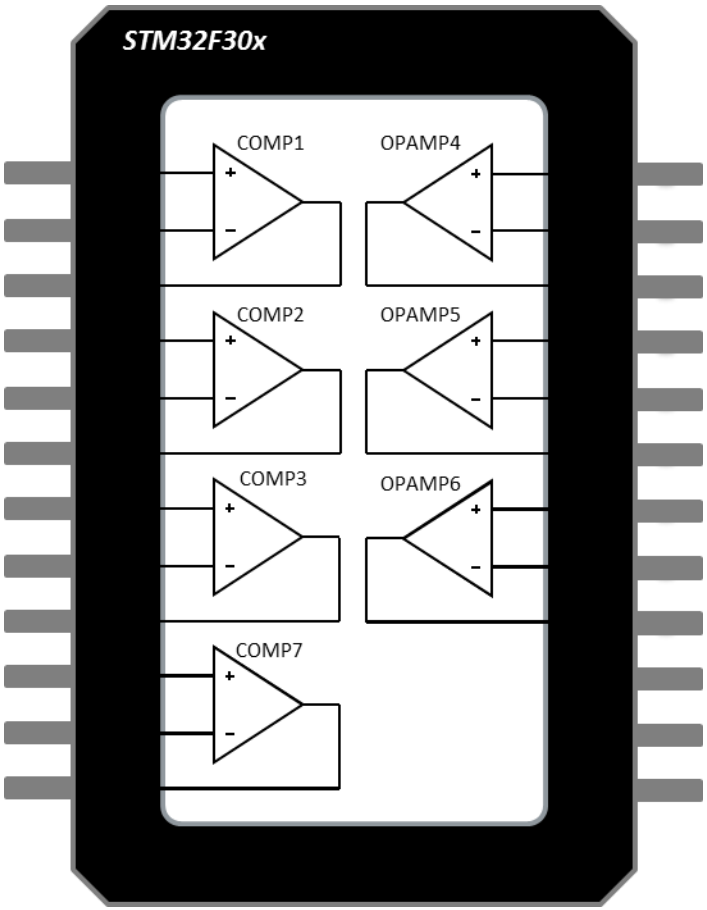


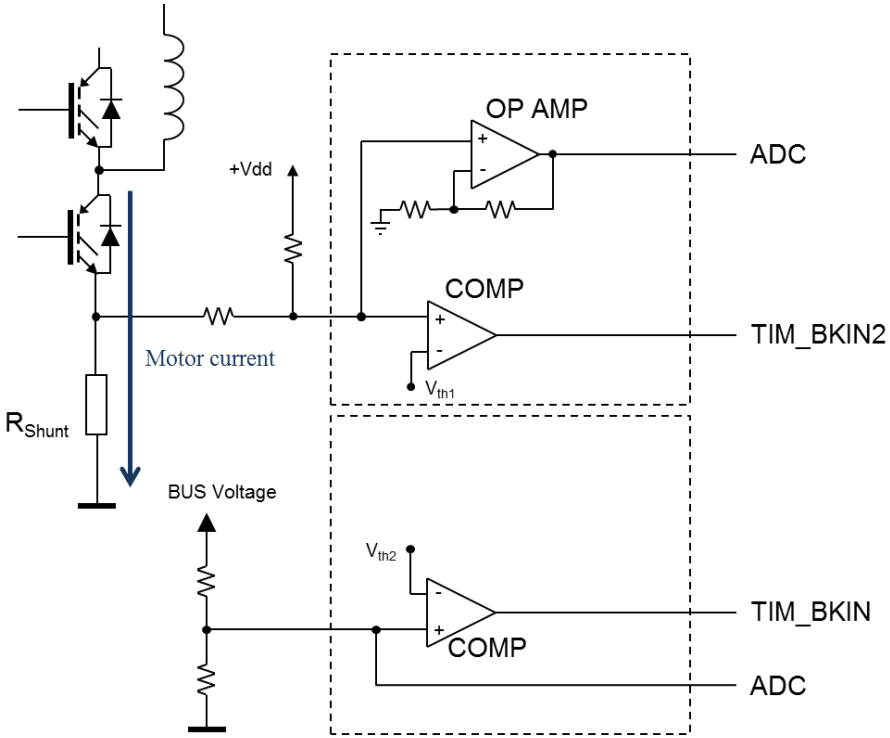
Internal gain & filter



Comparators

Up to seven fast comparators for fault protection





Characteristics

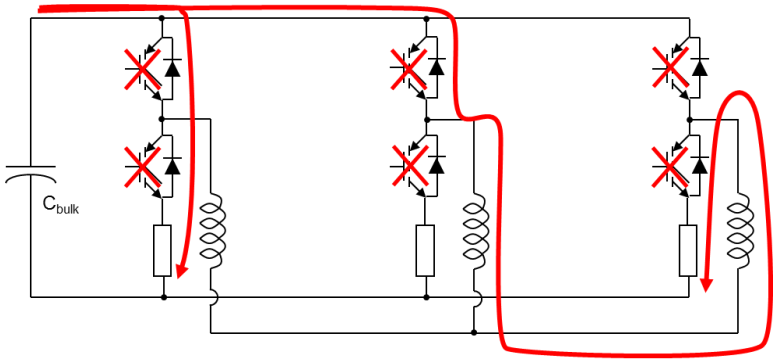
- 90ns propagation delay
- Rail-to-rail
- External or internal reference (DAC, 1.2V, 0.9V, 0.6V, 0.3V)
- Triggers Timer break inputs
- Registers lock

Emergency inputs

Different behaviors

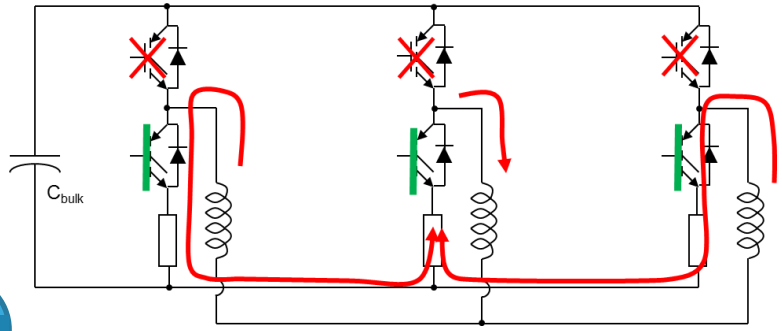
Over current protection

BKIN2 → PWM TIMER →



Over voltage protection

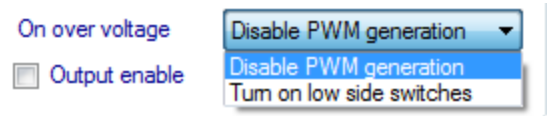
BKIN → PWM TIMER →



Characteristics

- Two different inputs programmable
- Digital filters
- Polarity
- Active on CSS, PDV, SRAM parity error, Core Hard fault

ST MC Workbench



MC library and Workbench support to F3 analog

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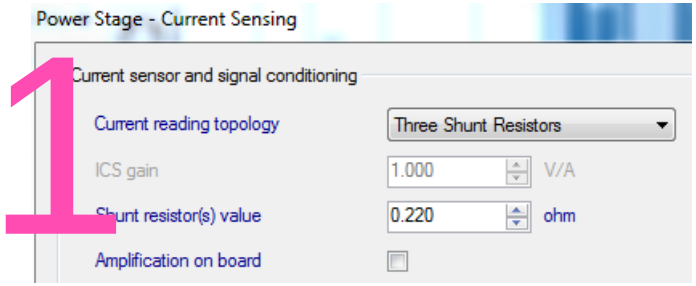
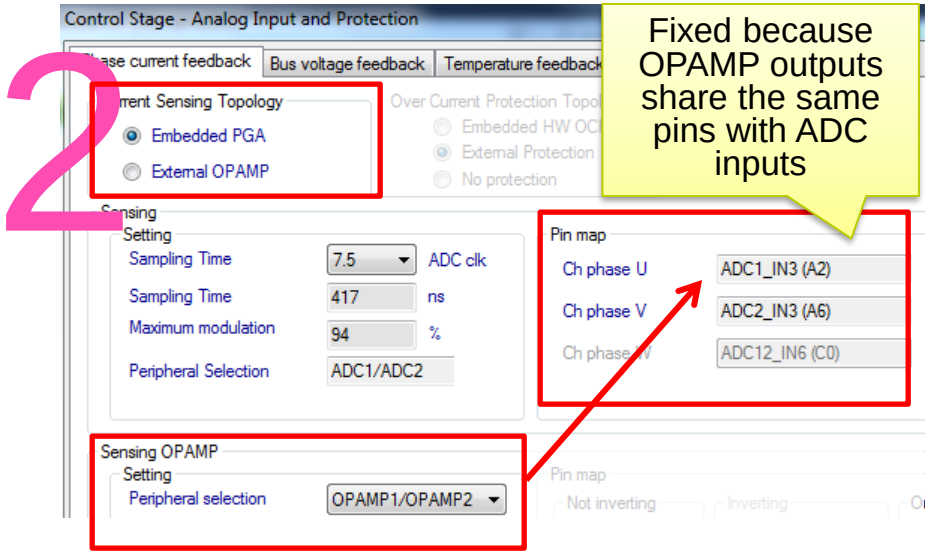
PGA, 3shunt current sensing

- For a 3shunt current sensing topology, a new feature implemented in MC library v5.x allows to commit two F3's PGA instead of three as it's usual.

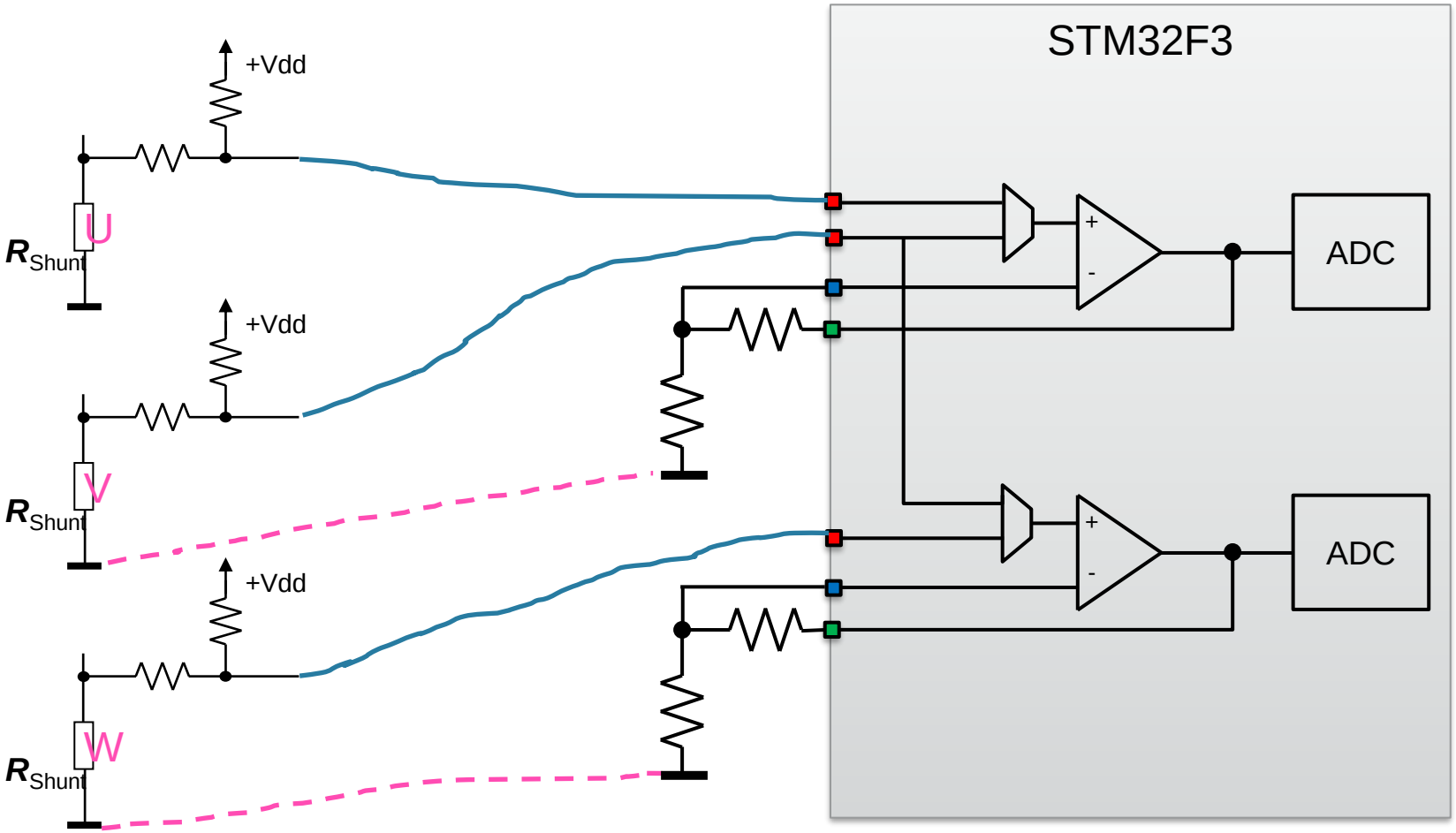
Micro	Available configurations	or
STM32F303	OPAMP1+ADC1 OPAMP2+ADC2	OPAMP3+ADC3 OPAMP4+ADC4
STM32F302	OPAMP1+ADC1 OPAMP2+ADC2	





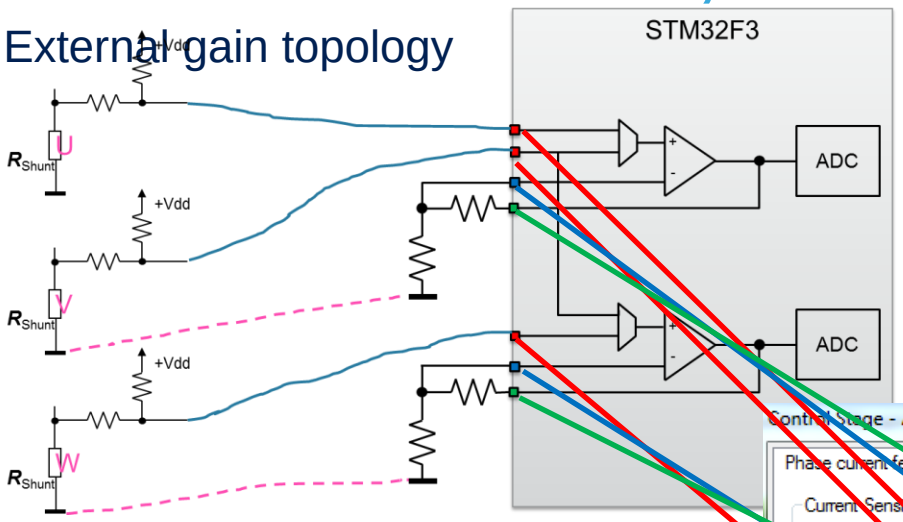
PGA, 3shunt current sensing

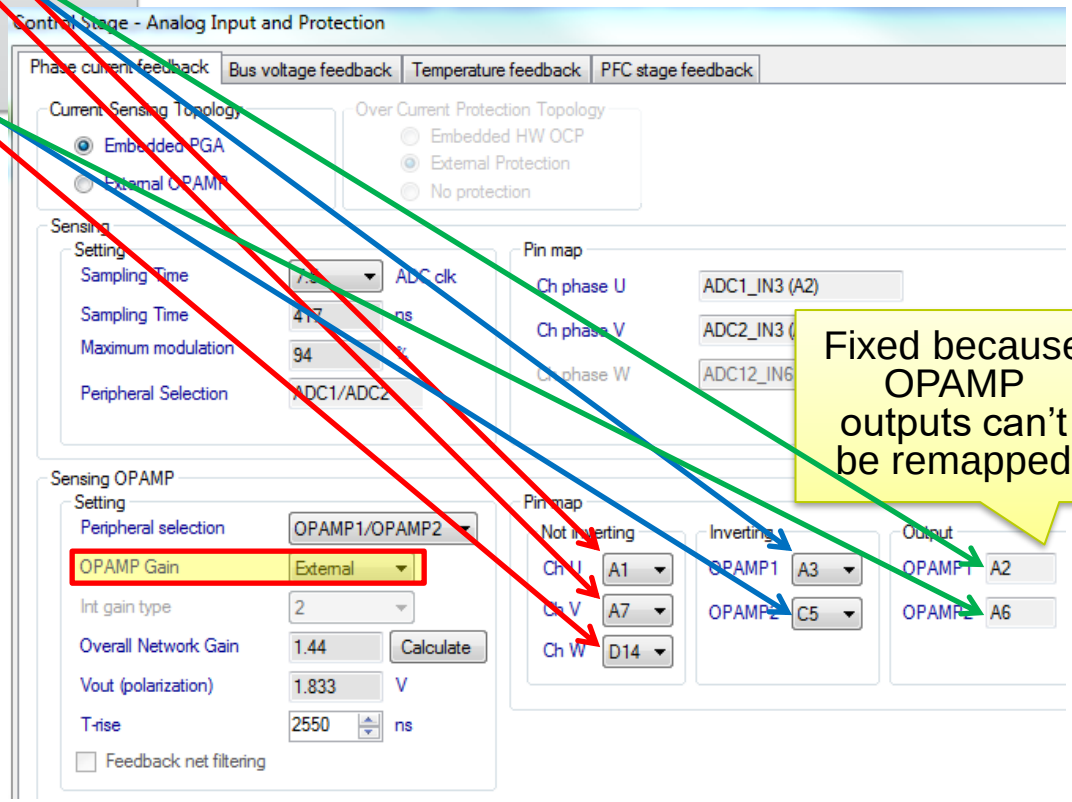
- External gain topology
- 7 mcu pins needed:
  - 3 non inverting; 2 inverting; 2 output



PGA, 3shunt current sensing

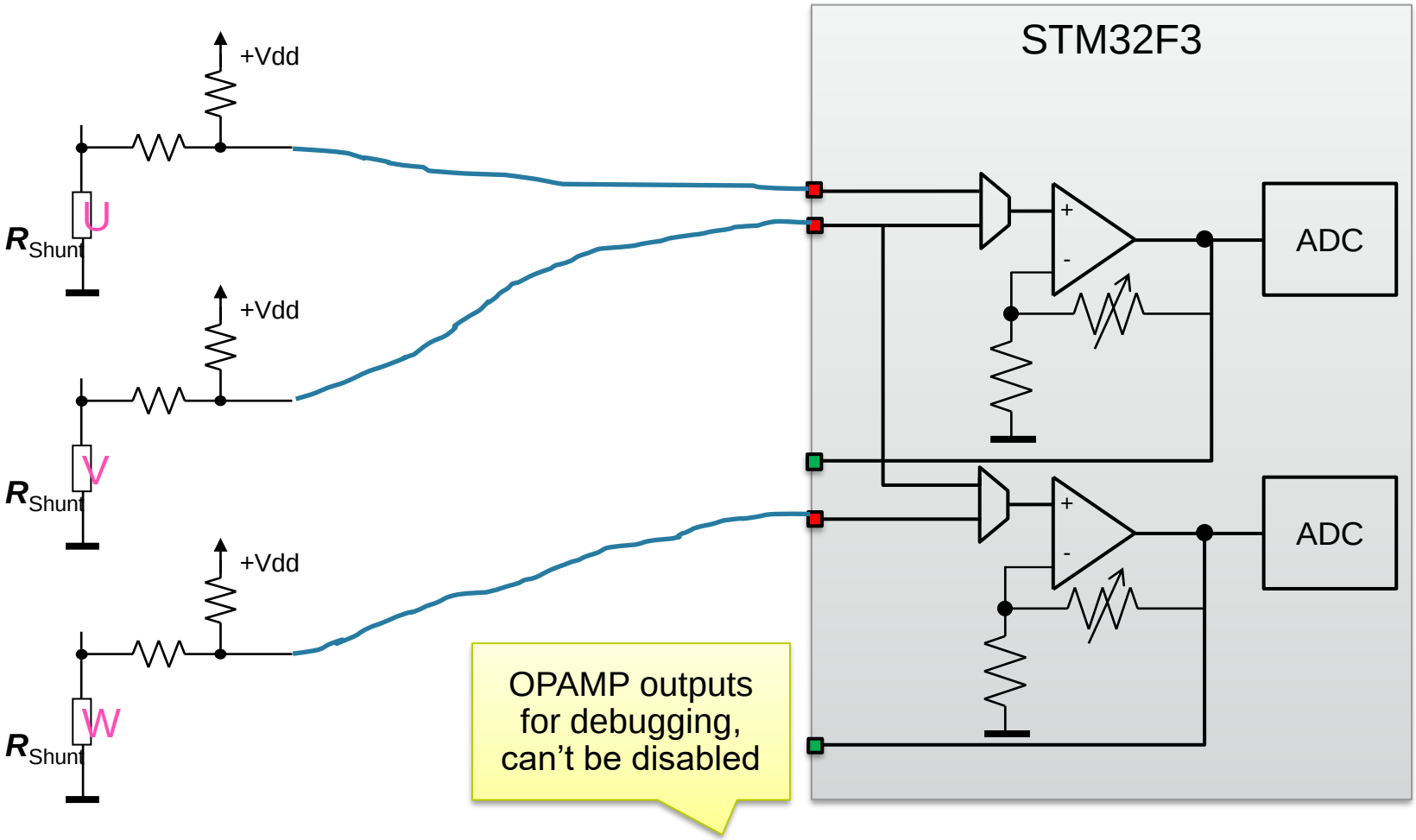
- External gain topology





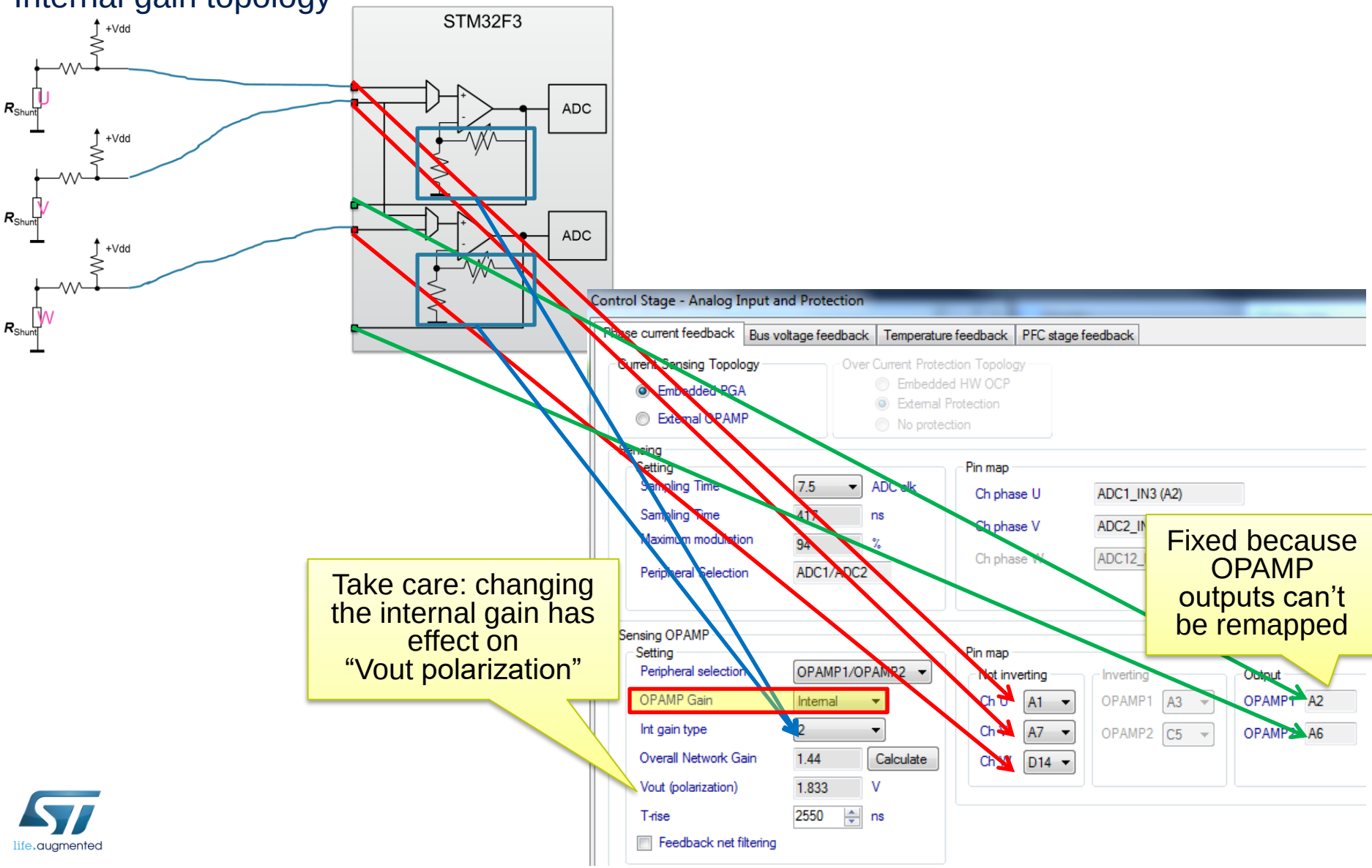
PGA, 3shunt current sensing

- Internal gain topology
- 5 mcu pins needed:
  - 3 non inverting; 2 output



PGA, 3shunt current sensing

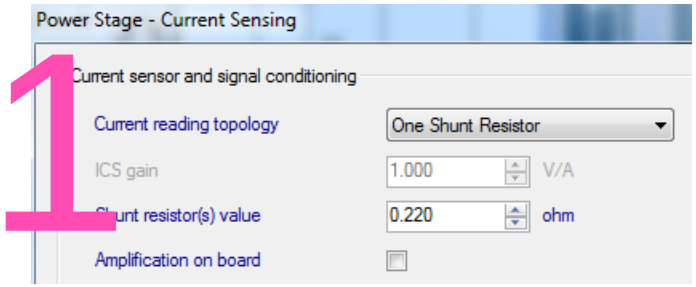
- Internal gain topology

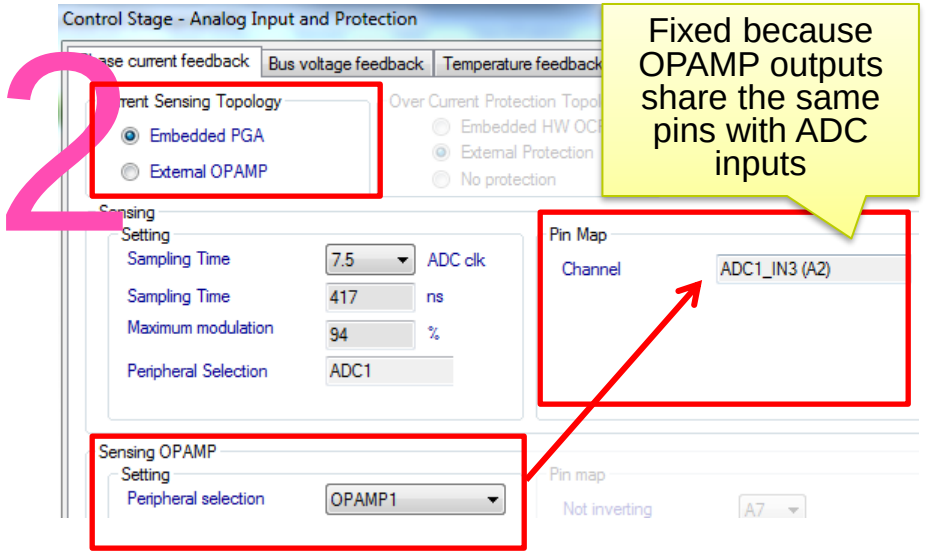


PGA, 1shunt current sensing

- For a 1shunt current sensing topology, each one of the OPAMP/ADC structures can be selected

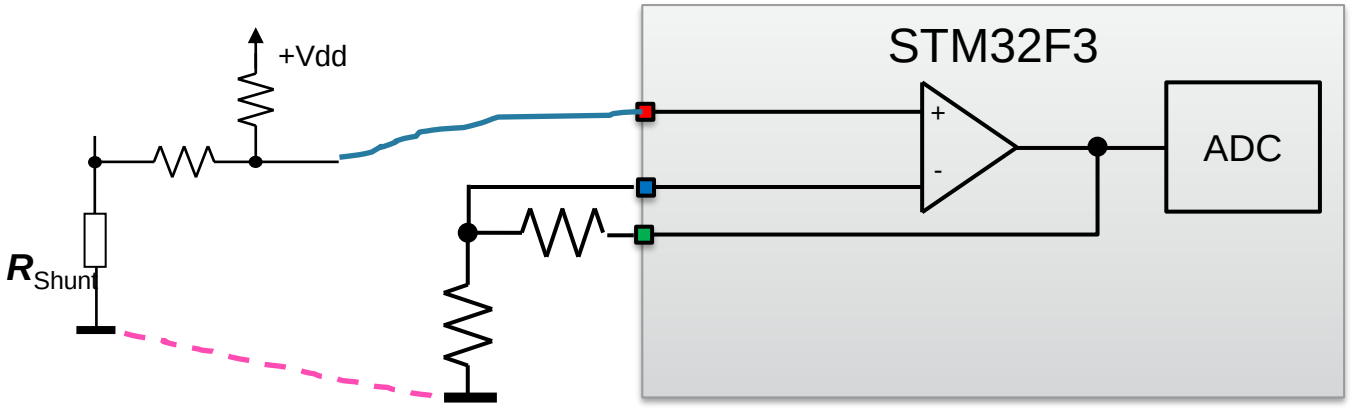
Micro	Available configurations	or	or	or
STM32F303	OPAMP1+ADC1	OPAMP2+ADC2	OPAMP3+ADC3	OPAMP4+ADC4
STM32F302	OPAMP1+ADC1	OPAMP2+ADC2		





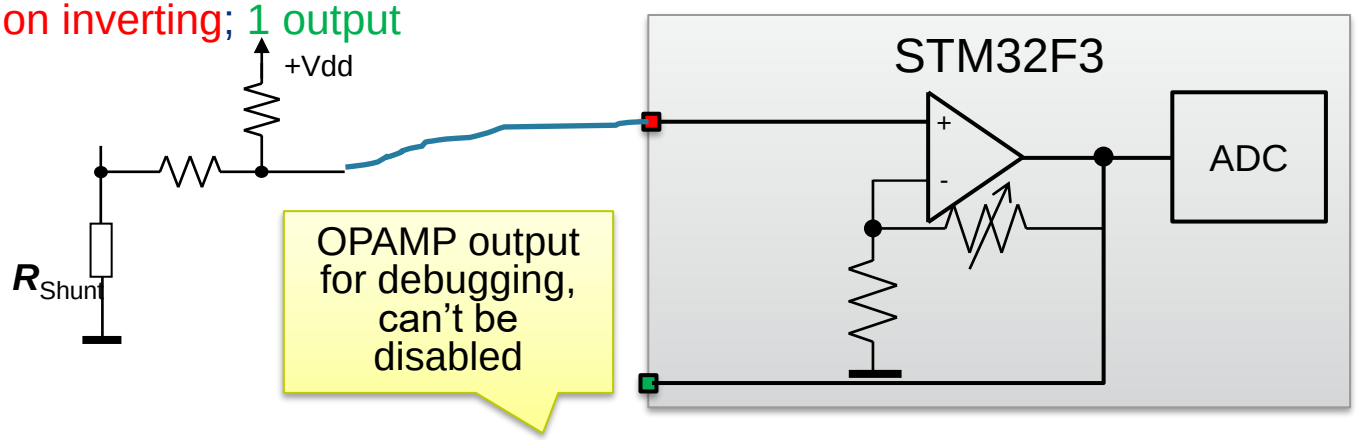
PGA, 1shunt current sensing

- External gain topology
- 3 mcu pins needed:
  - 1non inverting; 1 inverting; 1 output



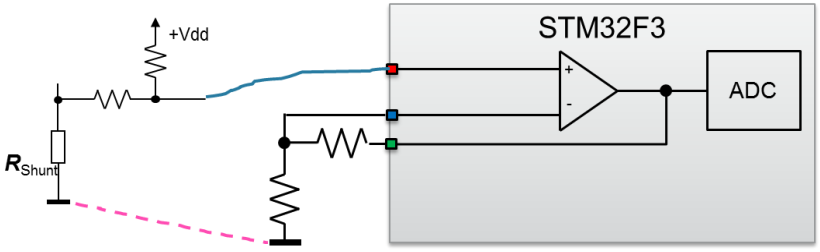
Internal gain topology

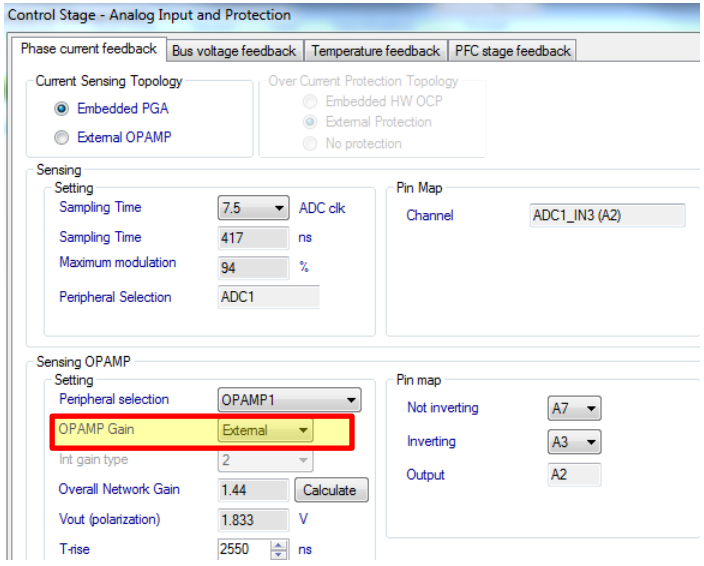
- 2 mcu pins needed:
  - 1non inverting; 1 output



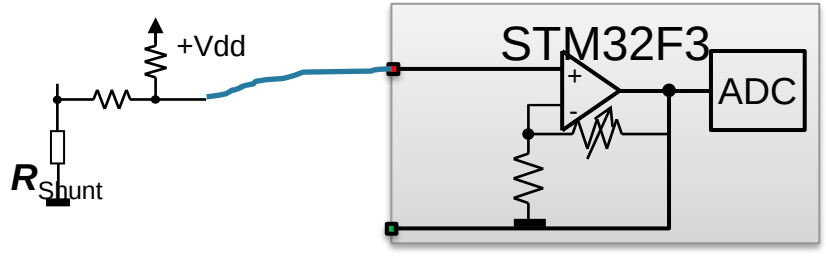
PGA, 1shunt current sensing

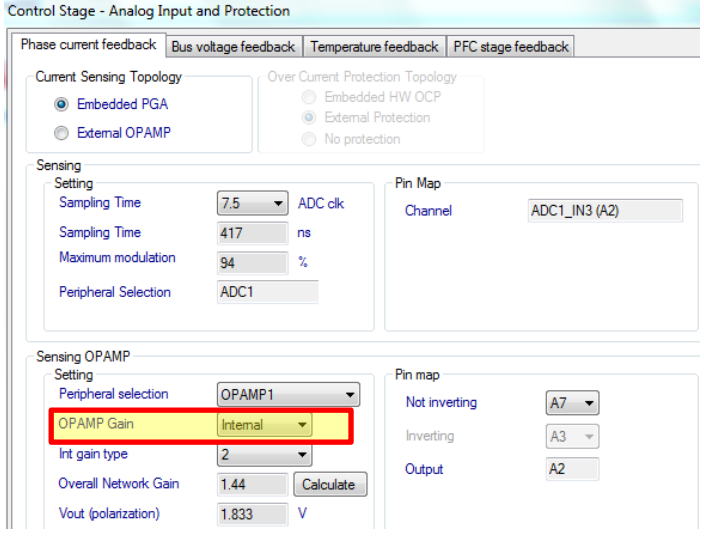
- External gain topology





- Internal gain topology





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PGA, dual motor control

- In a dual motor control project (STM32F303), all the configurations seen so far can be combined:
  - 3shunt and 1shunt
  - PGA and external OPAMP
  - Embedded comparators and external comparators

- For instance, configurations can range from

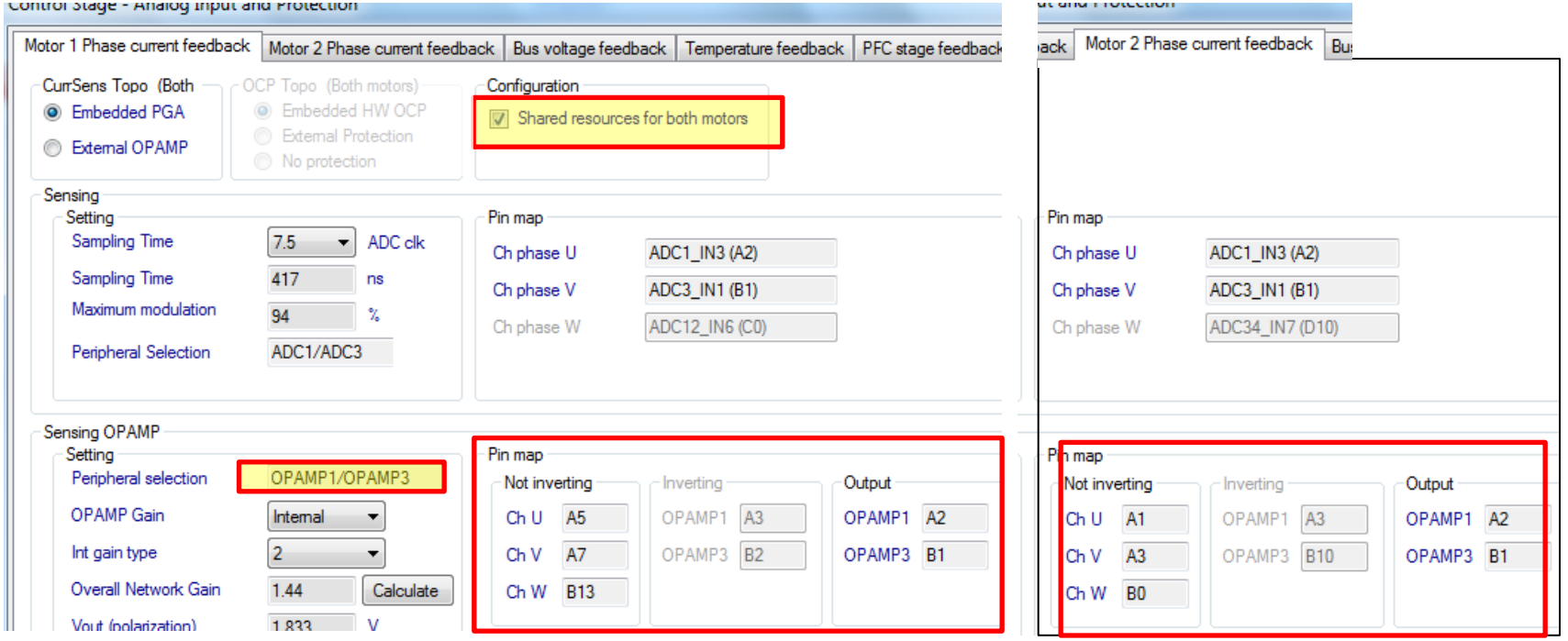
Motor	Topology	Resources for current sensing	Resources for OCP	Resources for OVP
First motor	3shunt	OPAMP1+ADC1 OPAMP2+ADC2	COMP1+2+3	COMP7 + ADC1
Second motor	3shunt	OPAMP3+ADC3 OPAMP4+ADC4	COMP4+5+6	ADC1

to

Motor	Topology	Resources for current sensing	Resources for OCP	Resources for OVP
First motor	1shunt	ADC2	COMP1	ADC1
Second motor	3shunt	OPAMP3+ADC3 OPAMP4+ADC4		ADC1

PGA, dual 3shunt with shared resources

- On top of this, an additional (optional) configuration of F3's resources has been dedicated to the dual 3shunt case
- The default choice assigns 4 OPAMP/ADC, i.e. 2 OPAMP/ADC for each motor
- The optional "Shared resource option" assigns 2 OPAMP/ADC in total, namely OPAMP1/ADC1 + OPAMP3/ADC3, sparing 2 OPAMP/ADC for other purposes
- The pinout assignment is fixed:



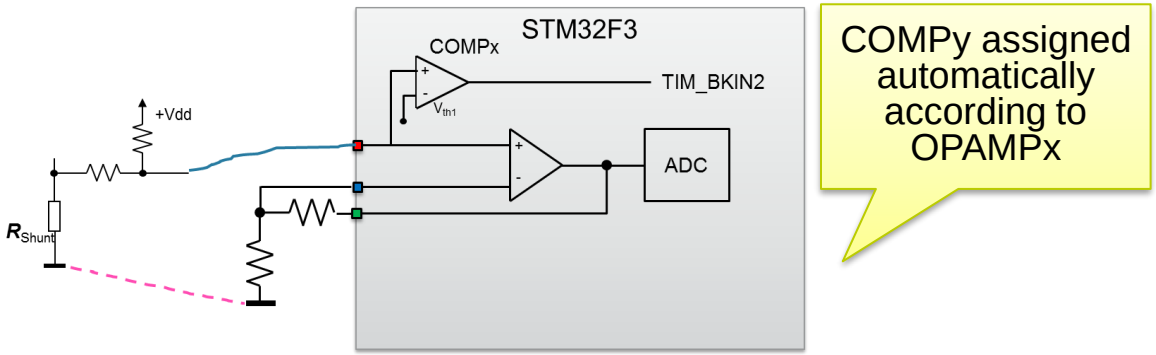
Comparators

WB settings

Overcurrent protection with embedded comparators

- The MC library v5.x allows F3's embedded comparators to serve as overcurrent protection (OCP) in 3shunt or 1shunt topologies.

- If both PGA for current sensing and embedded comparators for OCP are enabled, the resulting pin-out assignment is very convenient because same pins are used for both functions. Example in a 1shunt topology:

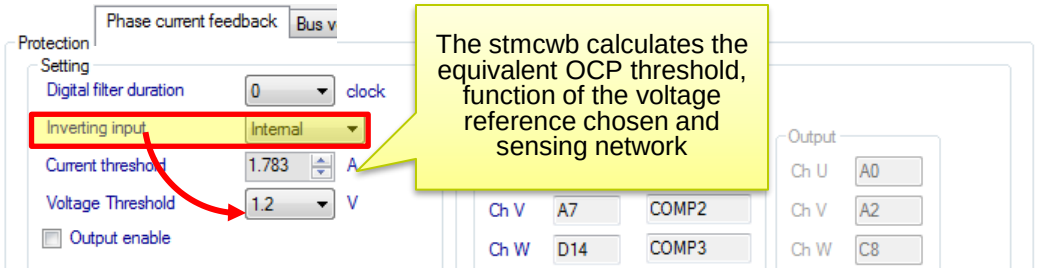


- Comparators can also be enabled in a configuration with external opamps

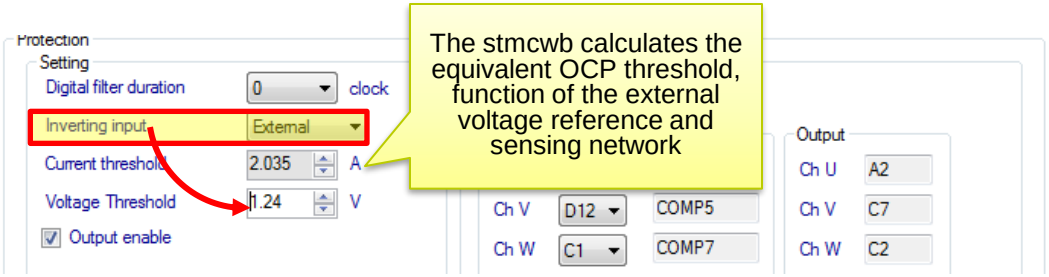
- On the other hand, the MC library doesn't allow to mix embedded and external comparators

Overcurrent protection with embedded comparators

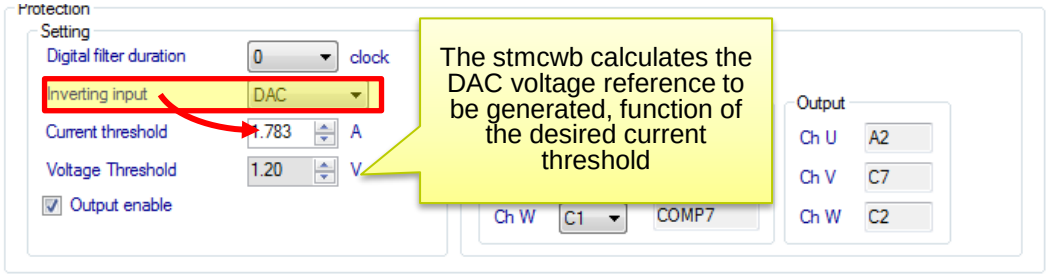
- Three different ways to set the OCP threshold:
  - Internal voltage references, sparing a I/O pin, but coarse definition



  - External voltage reference, 1 I/O pin (PA4), fine definition

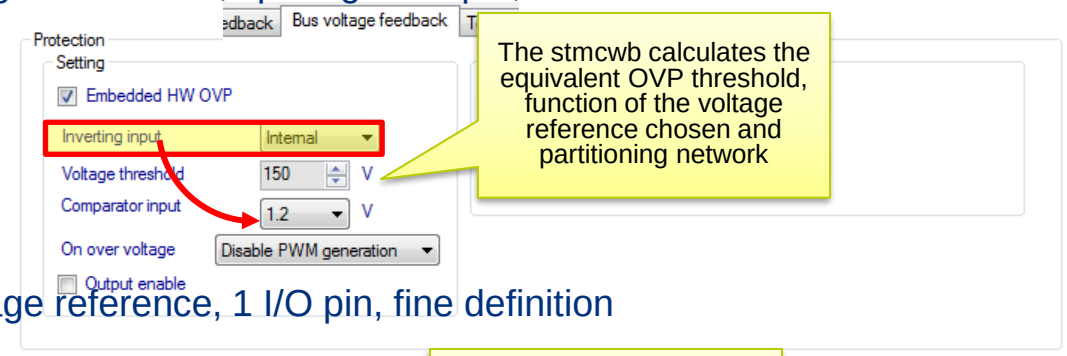


  - DAC channel, 1 I/O pin (to be defined in the DAC dialog window), fine definition

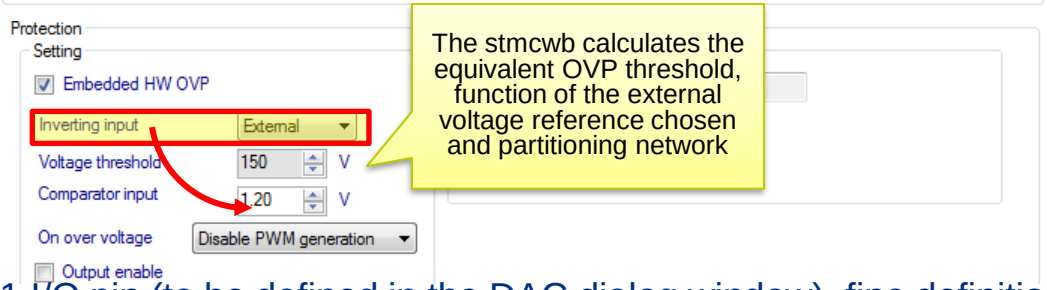


Overvoltage protection with embedded comparators

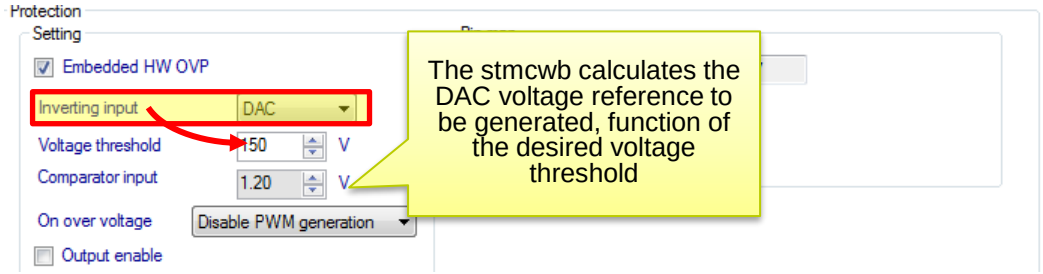
- Three different ways to set the OVP threshold:
  - Internal voltage references, sparing a I/O pin, but coarse definition



  - External voltage reference, 1 I/O pin, fine definition



  - DAC channel, 1 I/O pin (to be defined in the DAC dialog window), fine definition



Thanks